PXIe-5423

PXIe-5423

Contents

PXIe-5423 Specifications

These specifications apply to the one-channel and two-channel PXIe-5423.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

The following characteristic specifications describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Conditions

All specifications are valid under the following conditions unless otherwise noted:

- Signals terminated with 50 Ω to ground
- Load impedance set to 50 Ω
- Amplitude set to 2.4 V_{pk-pk}
- Analog Path property or NIFGEN_ATTR_ANALOG_PATH attribute set to Main (default)

- Reference Clock set to **Onboard Reference Clock**

Warranted and typical specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 0 °C to 55 °C
- 15-minute warm-up time before operation
- Self-calibration performed after instrument is stable
- External calibration cycle maintained and valid
- PXI Express chassis fan speed set to HIGH, foam fan filters removed if present, and empty slots contain PXI chassis slot blockers and filler panels

Analog Output

Number of channels[1]	1 or 2
Output type	Referenced single-ended
Connector type	SMA
DAC resolution	16 bits
Amplitude range[2], in 0.16 dB steps	
50 Ω load	0.00775 V_{pk-pk} to 12 V_{pk-pk}
Open load	0.0155 V_{pk-pk} to 24 V_{pk-pk}
Offset range	±50% of **Amplitude Range** (V_{pk-pk})[3]
Offset resolution	16-bit full-scale range
DC accuracy[4]	

Within ±5 °C of self-calibration temperature	±0.35% of **Amplitude Range** ± 0.35% of **Offset Requested** ± 500 µV, warranted[5]
0 °C to 55 °C	±0.55% of **Amplitude Range** ± 0.55% of **Offset Requested** ± 500 µV, typical

AC amplitude accuracy[6] (within ±5 °C of self-calibration temperature)	±1.0% ± 1 $mV_{pk\text{-}pk}$, warranted
Output impedance	50 Ω
Load impedance	Output waveform is compensated for user-specified impedances
Output coupling (ground referenced)	DC
Output enable[7]	Software-selectable
Maximum output overload[8]	±12 $V_{pk\text{-}pk}$ from a 50 Ω source
Waveform summing	Supported[9]

Standard Function

Sine Waveform

Frequency range	0 MHz to 40 MHz
Frequency step size	2.84 µHz

Table 1. Passband Flatness[10]

Sine Frequency	Passband Flatness (dB), Warranted	
	0.06 V_{pk-pk} to 2.75 V_{pk-pk}	>2.75 V_{pk-pk}
1 MHz	±0.4	±0.4
10 MHz	±0.4	±0.4
20 MHz	±0.4	±0.6
40 MHz[11]	±0.45	±0.8

Figure 1. Passband Flatness

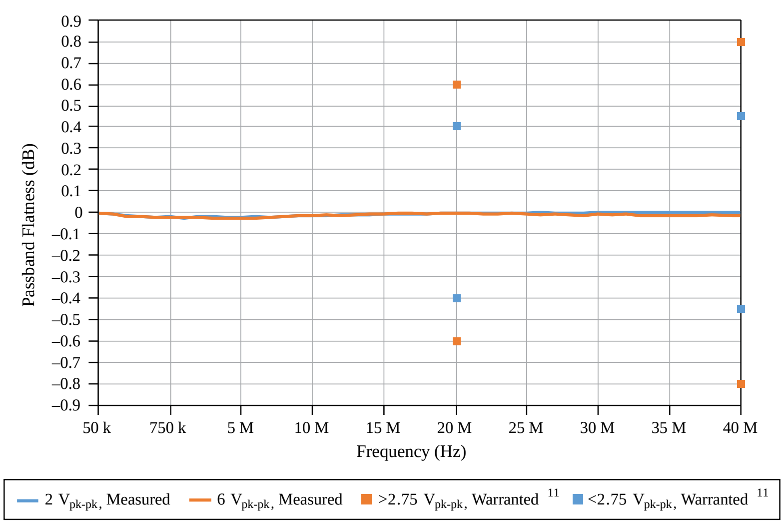


Table 2. Spurious-Free Dynamic Range (SFDR) with Harmonics[12]

Sine Frequency	SFDR with Harmonics (dBc), Measured		
	0.1 V_{pk-pk} to 1 V_{pk-pk}	1 V_{pk-pk} to 2.75 V_{pk-pk}	>2.75 V_{pk-pk}
1 MHz	62	76	77
3 MHz	62	74	63
5 MHz	61	74	58
10 MHz	61	69	52
20 MHz	61	63	44
30 MHz	59	60	40
40 MHz	55	58	35

Table 3. Spurious-Free Dynamic Range (SFDR) without Harmonics[12]

Sine Frequency	SFDR without Harmonics (dBc), Measured		
	0.1 V_{pk-pk} to 1 V_{pk-pk}	1 V_{pk-pk} to 2.75 V_{pk-pk}	>2.75 V_{pk-pk}
1 MHz	62	84	92
3 MHz	62	84	92
5 MHz	62	84	92
10 MHz	61	83	90
20 MHz	61	83	90
30 MHz	61	83	83
40 MHz	61	83	83

Table 4. Total Harmonic Distortion (THD)[13]

Sine Frequency	THD (dBc), Measured	
	0.1 V_{pk-pk} to 2.75 V_{pk-pk}	2.75 V_{pk-pk} to 12 V_{pk-pk}
1 MHz	79	76
3 MHz	73	62
5 MHz	72	56
10 MHz	68	49
20 MHz	61	43
30 MHz	58	39
40 MHz	55	35

Figure 2. 5 MHz Spectrum[14] at 0.6 V_{pk-pk}, Measured

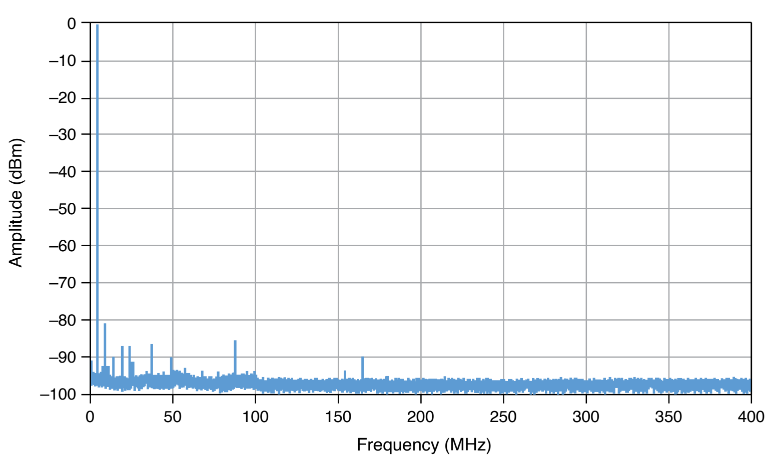


Figure 3. 10 MHz Spectrum[14] at 2 V_{pk-pk}, Measured

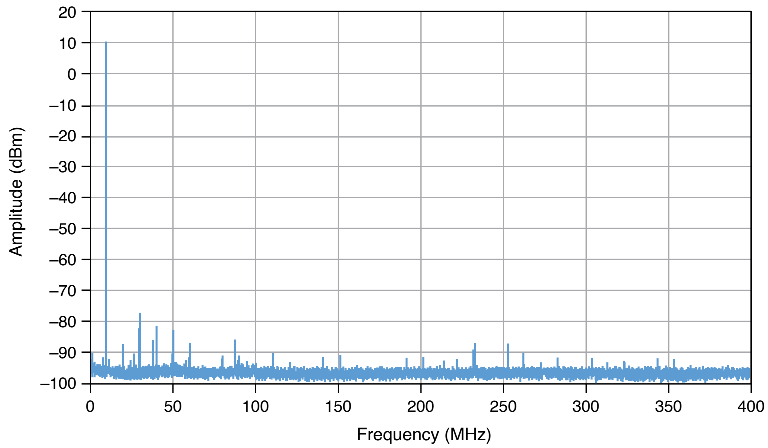


Figure 4. 1 MHz Spectrum[14] at 6.5 V_{pk-pk}, Measured

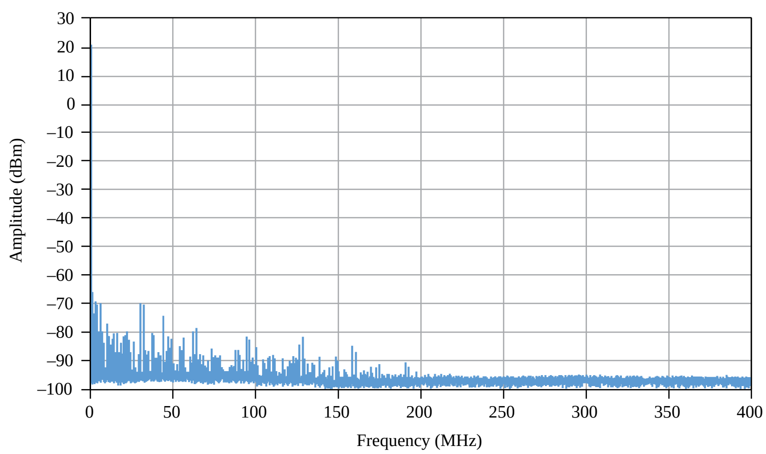
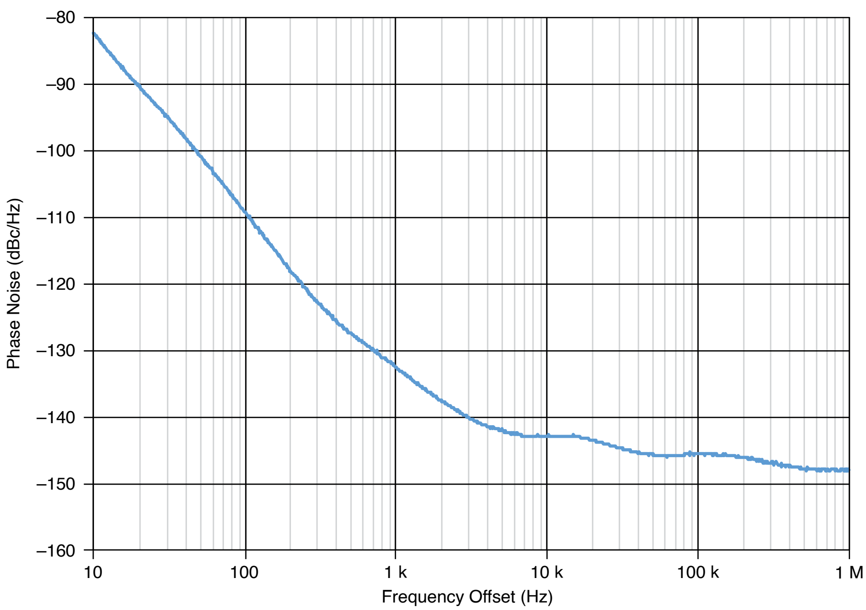


Table 5. Average Noise Density[15]

Amplitude	Average Noise Density, Typical	
	dBm/Hz	$\frac{nV}{\sqrt{Hz}}$
0.06 V_{pk-pk}	-154	3.9
0.1 V_{pk-pk}	-154	3.9
0.4 V_{pk-pk}	-150	5.8

Amplitude	Average Noise Density, Typical	
	dBm/Hz	$\frac{nV}{\sqrt{Hz}}$
1 $V_{pk\text{-}pk}$	-145	13
2 $V_{pk\text{-}pk}$	-141	20
4 $V_{pk\text{-}pk}$	-132	53
12 $V_{pk\text{-}pk}$	-125	107

Figure 5. Phase Noise[16], Measured



Jitter (RMS)[17]	214 fs

Square Waveform

Frequency range	0 MHz to 25 MHz
Frequency step size	2.84 µHz
Minimum on/off time[18]	17.6 ns

Duty cycle resolution	<0.001%
Rise/fall time[19]	9 ns, measured
Aberration	1.0%, measured
Jitter (RMS)[20]	2 ps, measured

Figure 6. Square Waveform Step Response at 2.75 $V_{pk\text{-}pk}$, Measured

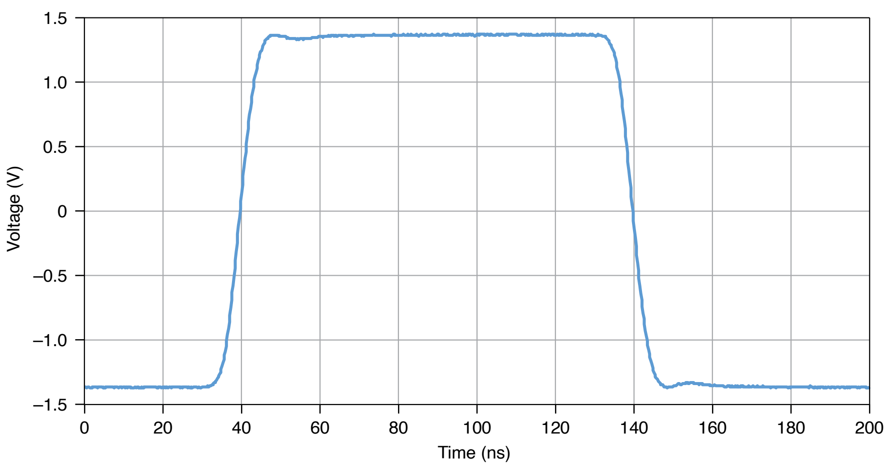
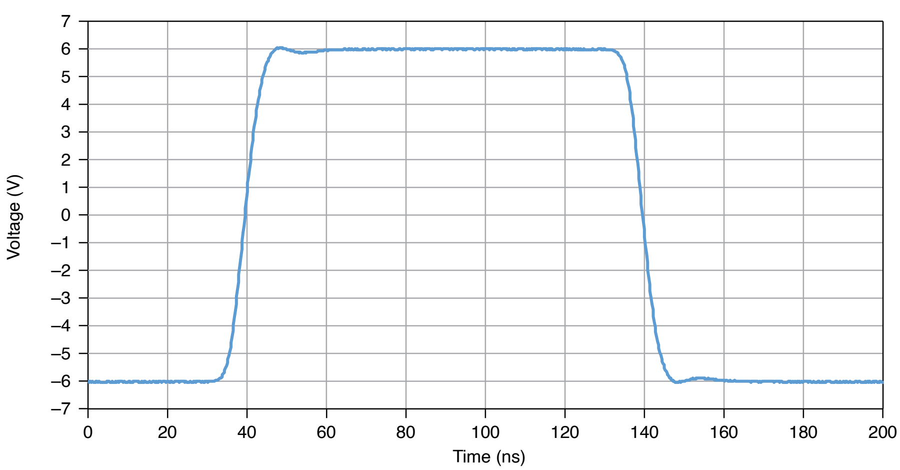


Figure 7. Square Waveform Step Response at 12 $V_{pk\text{-}pk}$, Measured



Ramp and Triangle Waveforms

Frequency range	0 MHz to 5 MHz

User-Defined Function

Frequency range	0 MHz to 40 MHz
Frequency step size	2.84 µHz
Waveform points	8,192
Step response rise time	7 ns, measured

Arbitrary Waveform

Waveform size	2 samples to 64,000,000 samples
User sample rate	
Digital filter enabled	5.6 µS/s to 200 MS/s
Digital filter disabled	3.125 MS/s to 200 MS/s
Waveform filters	
Digital filter enabled	**Bandwidth** = 0.2 * **User Sample Rate**
Digital filter disabled	No reconstruction image rejection
Minimum quantum size	1 sample
Rise time[21]	

Digital filter enabled	15.3 ns, measured
Digital filter disabled	8.4 ns, measured
Total onboard memory	128 MB per channel

Figure 8. Magnitude Response[22], Measured

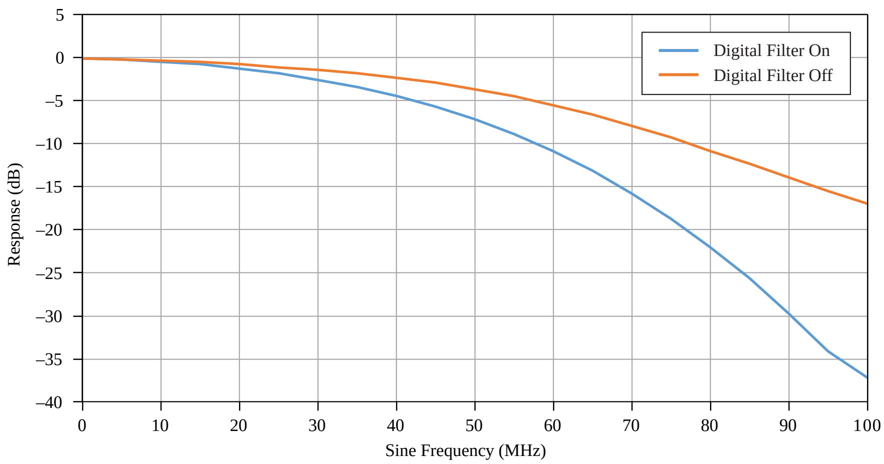


Figure 9. 10 MHz Single-Tone Spectrum[23], Measured

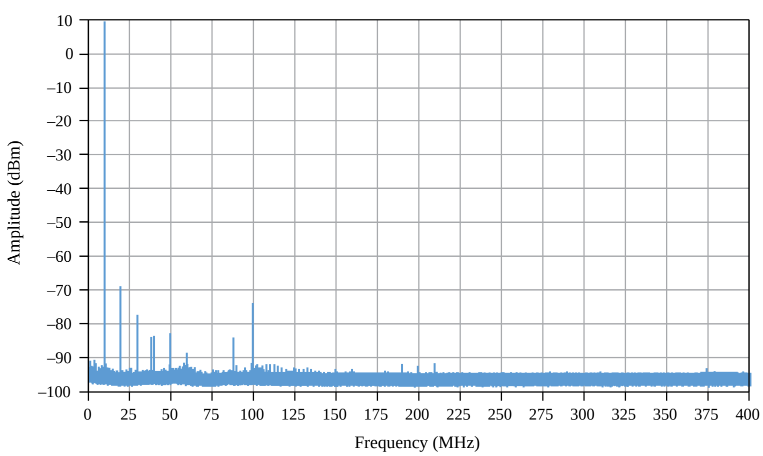
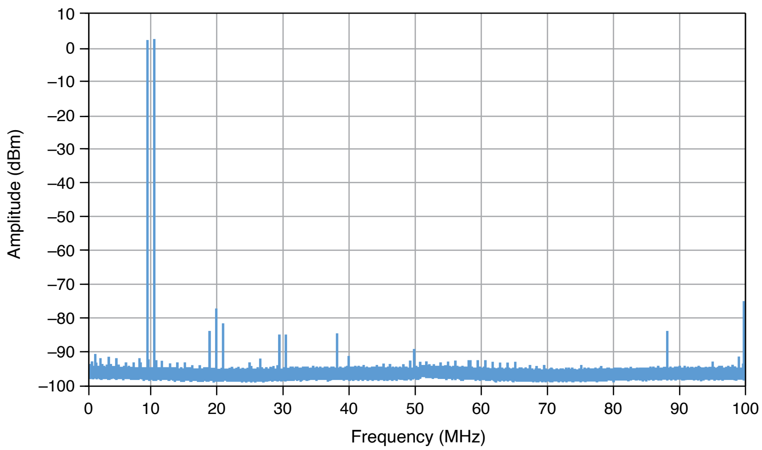


Figure 10. 9.5 MHz and 10.5 MHz Dual-Tone Spectrum[24], Measured



All Output Modes

Figure 11. Channel-To-Channel Crosstalk, Measured

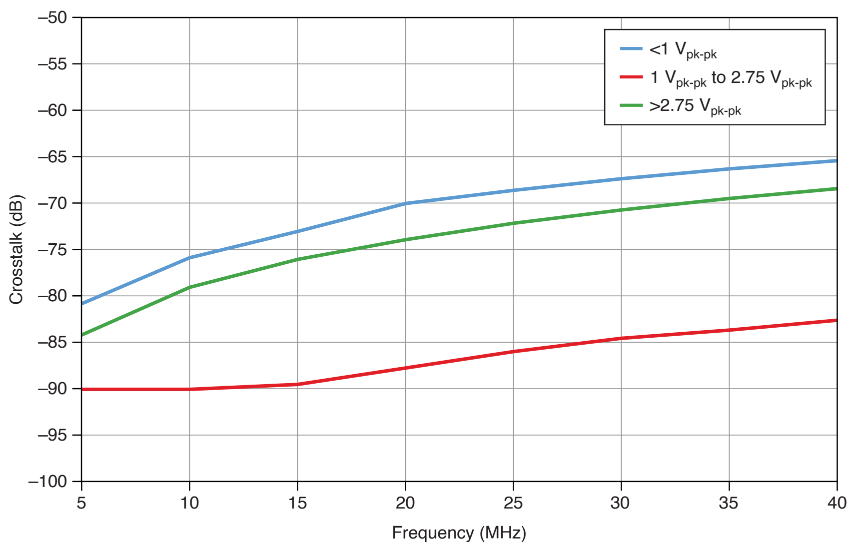
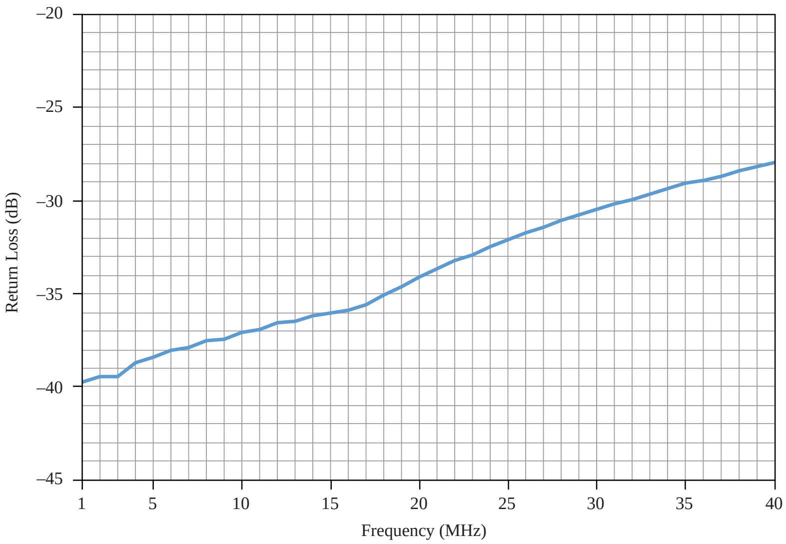


Figure 12. Return Loss, Measured



Clock

Reference Clock source	Internal PXIe_CLK100 (backplane connector)
Reference Clock frequency	100 MHz (<±25 ppm)
Sample Clock rate	800 MHz

Internal timebase accuracy[25]

Initial calibrated accuracy	1.5 ppm, warranted
Time drift[26]	1 ppm per year, warranted
Accuracy	**Initial Calibrated Accuracy** ± **Time Drift**, warranted

Synchronization

Channel-to-channel skew, between the channels of a multichannel PXIe-5423[27]	
<2.75 Vpk-pk	±110 ps
>2.75 Vpk-pk	±275 ps

Note The channels of a multichannel PXIe-5423 are automatically synchronized when they are in the same NI-FGEN session.

Synchronization with the NI-TClk API[28]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5423 and NI-FGEN.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PXIe-5423 modules using NI-TClk[29]	
NI-TClk synchronization without manual adjustment[30]	
Skew, peak-to-peak[31]	300 ps, typical
Jitter, peak-to-peak[32]	125 ps, typical
NI-TClk synchronization with manual adjustment[30]	
Skew, average	<10 ps

Jitter, peak-to-peak[32]	5 ps
Sample Clock delay/adjustment resolution	3.8E(-6) * **Sample Clock period** For example, at 100 MS/s, 3.8E(-6) * (1/100 MS/s) = 38 fs.

PFI I/O

Number of terminals	10
Connector type	
PFI 0 and PFI 1	SMA
AUX 0/PFI <0..7>	MHDMR
Logic level	3.3 V
Maximum input voltage	+5 V
V_{IH}	2 V
V_{IL}	0.8 V
Frequency range	0 MHz to 25 MHz
PFI-to-channel crosstalk	-80 dBc, measured

Trigger

Sources/destinations	PFI <0..1> (SMA front panel connectors)

	AUX 0/PFI <0..7> (MHDMR front panel connector) PXI_Trig <0..7> (backplane connector)
Supported triggers	Start Trigger Script Trigger
Trigger type	Rising edge
Trigger modes[33]	Single Continuous Stepped Burst
Input impedance (DC)	>100 kΩ

Marker

Destinations	PFI <0..1> (SMA front panel connectors) AUX 0/PFI <0..7> (MHDMR front panel connector) PXI_Trig <0..7> (backplane connector)
Pulse width	200 ns

Marker to output skew

PFI <0..1> and AUX 0/PFI <0..7>	±2 ns

PXI_Trig <0..7>	±20 ns
Maximum number of marker outputs per waveform	4

Calibration

Self-calibration	An onboard reference is used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 2 minutes to complete.
External calibration	External calibration calibrates the TCXO, voltage reference, and DC gain and offset. Appropriate constants are stored in nonvolatile memory.
Calibration interval	Specifications valid within 2 years of external calibration
Warm-up time[34]	15 minutes

Power

Current	
+3.3 V rail	2.3 A
+12 V rail	1.8 A
Total power	29 W

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)

Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random vibration

Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Physical

Dimensions	21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.) 3 U, one slot, PXI Express module

Weight	
One channel	369 g (13.0 oz)
Two channels	376 g (13.3 oz)

Bus interface	
Form factor	Gen 1 x4 module
Slot compatibility	PXI Express or hybrid

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions

- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Online Product Certification section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Minimize Our Environmental Impact** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

> **EU Customers** At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

> **中国客户** National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

[1] Channels support independent waveform generation.

[2] Amplitude values assume the full scale of the DAC is utilized. NI-FGEN uses waveforms less than the full scale of the DAC to create amplitudes smaller than the minimum value.

[3] For example, a 5.5 $V_{pk\text{-}pk}$ range equals ±2.75 V maximum offset. Offset range has a limitation of ±12 V absolute signal swing into high-impedance loads (**Amplitude** + |**Offset**| ≤ 12 V into high-impedance load or 6 V into 50 Ω load).

[4] Terminated with high-impedance load (load impedance set to 1 MΩ). The analog path is calibrated for amplitude, gain, and offset errors.

[5] Where **Amplitude Range** is the requested amplitude in V_{pk-pk}. For example, a DC signal with an amplitude range of 16 V_{pk-pk} and offset of 1.5 will calculate DC accuracy using the following equation: ±[(0.35% * 16 V) + (0.35% * 1.5 V) + 500 µV] = ±61.75 mV. The DC standard function always uses the 24 V_{pk-pk} amplitude range.

[6] With 50 kHz sine wave and terminated with high-impedance load.

[7] When the output path is disabled, the channel output is terminated to ground with a 50 Ω, 1 W resistor.

[8] No damage occurs if the analog output channels are shorted to ground indefinitely.

[9] The output terminals of multiple PXIe-5423 waveform generators can be connected together.

[10] Normalized to 50 kHz.

[11] With sine frequencies of 40 MHz and ambient temperatures above 45 °C, add ±0.015 dB/°C to the passband flatness specification.

[12] At amplitude of -1 dBFS with 0 V DC offset, measured from DC to 400 MHz, and limited to a -90 dBm spur at low amplitudes.

[13] At amplitude of -1 dBFS and measured from DC to the sixth harmonic.

[14] Noise floor is limited by the noise floor of the measurement device.

[15] At small amplitudes, average noise density is limited by a -154 dBm/Hz noise floor.

[16] With 40 MHz carrier and locked to the internal timebase with spurs removed.

[17] With 40 MHz carrier, integrated from 100 Hz to 100 kHz, and locked to the internal timebase.

[18] Used for calculating duty cycle limit:
Minimum Duty Cycle = (100% * **Minimum On Time**) ÷ T_{period}
and **Maximum Duty Cycle** = 100% - **Minimum Duty Cycle**. For more information about the relationship between minimum on/off time and duty cycle specifications, refer to ni.com.

[19] Rise time measured from 10% to 90%.

[20] Integrated from 10 Hz to 10 MHz using a 22 MHz square wave.

[21] At maximum user sample rate.

[22] Relative to 50 kHz and at 2 $V_{pk\text{-}pk}$ and maximum user sample rate.

[23] With the digital filter enabled and at -1 dBFS, 2 $V_{pk\text{-}pk}$, and 200 MS/s. Noise floor is limited by the noise floor of the measurement device.

[24] With the digital filter enabled and at -7 dBFS, 2 $V_{pk\text{-}pk}$, and 200 MS/s. Noise floor is limited by the noise floor of the measurement device.

[25] If locked to an external Reference Clock source, timebase accuracy is equal to the external Reference Clock accuracy.

[26] Where time drift starts at the latest external calibration date.

[27] With a 20 MHz sine wave and both channels configured with the same amplitude.

[28]

NI-TClk synchronization support for the PXIe-5423 was first available in NI-FGEN 18.1. NI-TClk installs with NI-FGEN.

[29] Specifications are valid for any number of PXIe-5423 modules installed in one chassis, with each PXIe-5423 module using a single NI-FGEN session and having all analog parameters set to identical values, and Sample Clock set to 100 MS/s. For

other configurations, including multi-chassis systems, contact NI Technical Support at ni.com/support.

30 Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.

31 Caused by clock and analog path delay differences.

32 Synchronization jitter is the variation in module alignment across calls to NI-TClk Synchronize.

33 In frequency list, arbitrary waveform, and arbitrary sequence output modes.

34 Warm up begins after the chassis is powered and the PXIe-5423 is recognized by the host and configured using NI-FGEN. Self-calibration is recommended following the warm-up time.