PCI/PXI-6230 Specifications

Contents

NI 6230 Specifications

Analog Input

Number of channels	4 differential or 8 single ended
Channel type	Voltage input
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the AI Absolute Accuracy section
Sample rate Single channel maximum Minimum	 250 kS/s 0 S/s
Timing resolution	50 ns
Timing accuracy	50 ppm of sample rate
Input coupling	DC
Input range	±0.2 V, ±1 V, ±5 V, ±10 V
Maximum working voltage for analog inputs	Refer to the Maximum Working Voltage section

CMRR (DC to 60 Hz)	95 dB (with respect to AI GND)
Input impedance **Device on** AI+ to AI GND AI- to AI GND **Device off** AI+ to AI GND AI- to AI GND	 >10 GΩ in parallel with 100 pF >10 GΩ in parallel with 100 pF 820 Ω 820 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz) Adjacent channels Non-adjacent channels	 -75 dB -90 dB
Small signal bandwidth (-3 dB)	700 kHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	DMA (scatter-gather), interrupts, programmed I/O
Overvoltage protection (AI <0..7> with respect to AI GND) Device on	 ±25 V for up to two AI pins

Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20 mA maximum/AI pin

Settling Time for Multichannel Measurements

Accuracy, full scale step, all ranges	
±90 ppm of step (±6 LSB)	4 µs convert interval
±30 ppm of step (±2 LSB)	5 µs convert interval
±15 ppm of step (±1 LSB)	7 µs convert interval

Typical Performance Graphs

Figure 1. Settling Error versus Time for Different Source Impedances

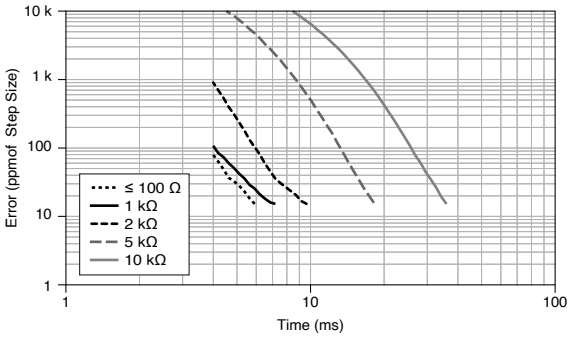


Figure 2. AI Small Signal Bandwidth

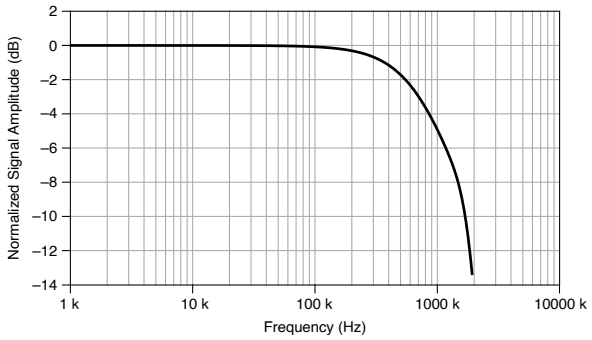


Figure 3. AI CMRR to Earth Ground

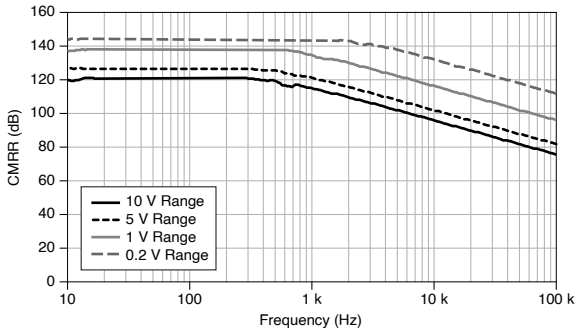
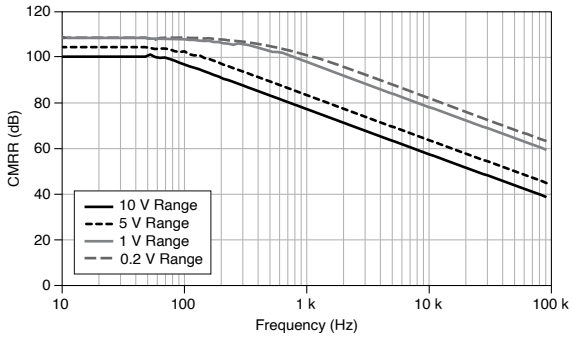


Figure 4. AI CMRR to AI GND



AI Absolute Accuracy

Note Accuracies listed are valid for up to one year from the device external calibration.

Table 1. AI Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)	Sensitivity (µV)
10	-10	75	20	57	244	3,100	97.6
5	-5	85	20	60	122	1,620	48.8
1	-1	95	25	79	30	360	12.0
0.2	-0.2	135	80	175	13	112	5.2

Note Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Gain tempco	25 ppm/°C
Reference tempco	5 ppm/°C
INL error	76 ppm of range

AI Absolute Accuracy Equation

AbsoluteAccuracy = **Reading** · **(GainError)** + **Range** · **(OffsetError)** + **NoiseUncertainty**

- **GainError** = **ResidualAIGainError** + **GainTempco** · **(TempChangeFromLastInternalCal)** + **ReferenceTempco** · **(TempChangeFromLastExternalCal)**
- **OffsetError** = **ResidualAIOffsetError** + **OffsetTempco** · **(TempChangeFromLastInternalCal)** + **INLError**

- **NoiseUncertainty** = $\frac{\text{Random Noise} \cdot 3}{\sqrt{100}}$ for a coverage factor of 3 σ and averaging 100 points.

AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- TempChangeFromLastExternalCal = 10 °C
- TempChangeFromLastInternalCal = 1 °C
- number_of_readings = 100
- CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- GainError = 75 ppm + 25 ppm · 1 + 5 ppm · 10 = 150 ppm
- OffsetError = 20 ppm + 57 ppm · 1 + 76 ppm = 153 ppm
- NoiseUncertainity = $\frac{244\ \mu V \cdot 3}{\sqrt{100}}$ = 73 µV
- AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainity = 3,100 µV

Analog Output

Number of channels	4
Channel type	Voltage output
DAC resolution	16 bits
DNL	±1 LSB

Monotonicity	16 bit guaranteed
Maximum update rate	
1 channel	500 kS/s
2 channels	450 kS/s per channel
3 channels	425 kS/s per channel
4 channels	400 kS/s per channel
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Output range	±10 V
Output coupling	DC
Output impedance	0.4 Ω
Output current drive	±5 mA
Overdrive protection	±25 V
Overdrive current	10 mA
Power-on state	±20 mV
Power-on glitch[1]	±2 V for 2 ms
Power-off glitch[2]	±100 mV for 350 ms

Output FIFO size	8,191 samples shared among channels used
Data transfers	DMA (scatter-gather), interrupts, programmed I/O
AO waveform modes	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full-scale step, 15 ppm (1 LSB)	6 µs
Slew rate	15 V/µs
Glitch energy	
Magnitude	100 mV
Duration	3 µs

AO Absolute Accuracy

Absolute accuracy at full-scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration.

Note Accuracies listed are valid for up to one year from the device external calibration.

Table 4. AO Absolute Accuracy

Nominal Range Positive Full Scale (V)	Nominal Range Negative Full Scale (V)	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Absolute Accuracy at Full Scale (µV)
10	-10	90	10	40	5	3,230

Reference tempco	5 ppm/°C
INL error	128 ppm of range

AO Absolute Accuracy Equation

AbsoluteAccuracy = **OutputValue** · **(GainError)** + **Range** · (**OffsetError**)

- **GainError** = **ResidualGainError** + **GainTempco** · (**TempChangeFromLastInternalCal**) + **ReferenceTempco** · (**TempChangeFromLastExternalCal**)
- **OffsetError** = **ResidualOffsetError** + **AOOffsetTempco** · **(TempChangeFromLastInternalCal)** + **INLError**

Digital I/O/PFI

Static Characteristics

Number of channels	10 total
Number of input channels	6 (PFI <0..5>/P0.<0..5>)
Number of output channels	4 (PFI <6..9>/P1.<0..3>)
Ground reference	D GND
Direction control	Fixed, lines are unidirectional
Input voltage protection	±20 V on up to two pins[3]

PFI/Port 1/Port 2 Functionality

PFI <0..5>/P0.<0..5>	Static digital input, timing input
PFI <6..9>/P1.<0..3>	Static digital output, timing output
Timing output sources	Many AI, AO, counter timing signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Digital Input Characteristics

Level	Min	Max
V_{IL} input low voltage	0 V	0.8 V
V_{IH} input high voltage	2 V	5.25 V
I_{IL} input low current (V_{in} = 0 V)	—	-10 µA
I_{IH} input high current (V_{in} = 5 V)	—	10 µA

Digital Output Characteristics

Table 4. Guaranteed Output Levels

Level	Voltage Level	Current Level
V_{OL}	0.4 V	7 mA
V_{OL}	0.6 V	10 mA
V_{OH}	2.8 V	-24 mA
V_{OH}	4.0 V	-6 mA

Maximum Operating Conditions

Level	Minimum	Maximum
I_{OL} output low current P1.<0..3>	—	10 mA

Level	Minimum	Maximum
I_{OH} output high current P1.<0..3>	—	-24 mA

General-Purpose Counters/Timers

Number of counter/timers	2
Resolution	32 bits
Counter measurements	Edge counting, pulse, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	80 MHz, 20 MHz, 0.1 MHz
External base clock frequency	0 MHz to 20 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Routing options for inputs	Any input PFI, RTSI, PXI_TRIG, PXI_STAR, many internal signals
FIFO	2 samples
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer; interrupts; programmed I/O

Isolation Effects

Maximum propagation delay through isolator	
Digital inputs	35 ns
Digital outputs	45 ns
Propagation delay skew between channels (inputs and outputs)	15 ns

Frequency Generator

Number of channels	1
Base clocks	10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm

Output can be available on any output PFI or RTSI terminal.

Phase-Locked Loop (PLL)

Number of PLLs	1
Reference signal	PXI_STAR, PXI_CLK10, RTSI <0..7>
Output of PLL	80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer function	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down

Device-To-Device Trigger Bus

PCI	RTSI <0..7>[4]
PXI	PXI_TRIG <0..7>, PXI_STAR
Output selections	10 MHz Reference Clock, frequency generator output, many internal signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Bus Interface

PCI or PXI	3.3 V or 5 V signal environment

PXI-6230 devices can be installed in PXI slots or PXI Express hybrid slots.

DMA channels	4, analog input, analog output, counter/timer 0, counter/timer 1

Power Requirements

Current draw from bus during no-load condition	
+5 V	0.5 A
+12 V	20 mA
Current draw from bus during AI and AO overvoltage condition	
+5 V	0.75 A
+12 V	20 mA

Physical Characteristics

Printed circuit board dimensions	
PCI	9.7 cm × 15.5 cm (3.8 in. × 6.1 in.)
PXI	Standard 3U PXI
Weight	
PCI	110 g (3.8 oz)
PXI	150 g (5.2 oz)
I/O connector	37-pin D-SUB

Calibration

Recommended warm-up time	15 minutes

Calibration interval	1 year

Maximum Working Voltage

Connect only voltages that are below these limits.

Channel-to-earth ground[5]	
Continuous	≤30 Vrms/60 VDC Measurement Category I
Withstand	≤840 Vrms/1,200 VDC, verified by a 5 s dielectric withstand test
Channel-to-bus[6]	
Continuous	≤30 Vrms/60 VDC Measurement Category I
Withstand	≤1,400 Vrms/1,950 VDC, verified by a 5 s dielectric withstand test
Analog channel-to-AI GND or AO GND (in the following figure, $\|V_a - V_c\|$)	≤11 V, Measurement Category I
Digital channel-to-D GND (in the following figure, $\|V_b - V_c\|$)	≤5.25 V, Measurement Category I

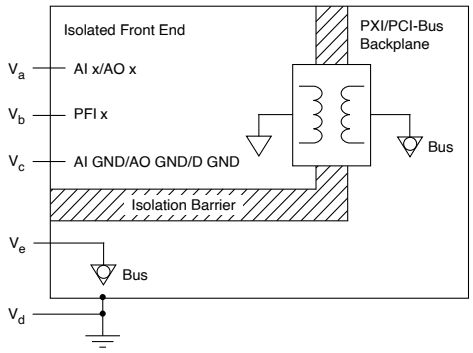
Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.

Caution This device is rated for Measurement Category I and the voltage across the isolation barrier is limited to no greater than 30 Vrms/60 VDC/ 42.4 V_{pk} continuous. These test and measurement circuits are not

> intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

The following figure illustrates the safety voltages specifications.

Figure 5. NI 6230 Safety Voltages



Environmental

Operating environment	
Ambient temperature range	0 to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)
Storage environment	
Ambient temperature range	-40 to 70 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.)
Relative humidity range	5% to 95% noncondensing (Tested in accordance with IEC-60068-2-56.)

Maximum altitude	2,000 m
Pollution Degree	2

Indoor use only.

Shock and Vibration (PXI Only)

Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

CE Compliance CE

- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

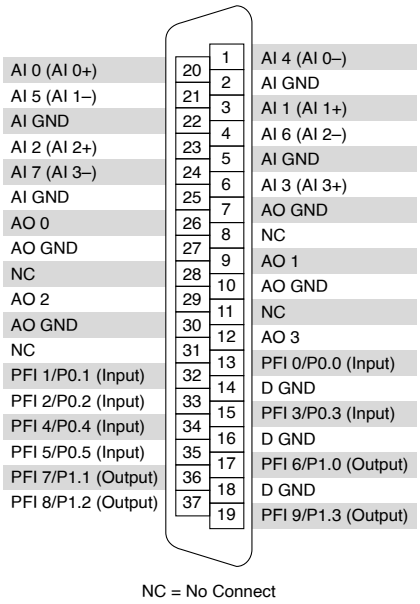
电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/

rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Device Pinout

Figure 6. NI PCI/PXI-6230 Pinout



NC = No Connect

[1] For the earlier version of the PCI-6230 (192233B-01), refer to the **NI 6230 Specifications** document, 371672A-01, January 2006 revision.

[2] When outputting 0 V on power down from the analog output channel.

[3] Stresses beyond those listed under **Input voltage protection** may cause permanent damage to the device.

[4] In other sections of this document, RTSI refers to RTSI <0..7> for the PCI devices or PXI_TRIG <0..7> for PXI devices.

[5] In the figure, $|V_a - V_d|$,$|V_b - V_d|$, and $|V_c - V_d|$.

[6] In the figure, $|V_a - V_e|$,$|V_b - V_e|$, and $|V_c - V_e|$.