PXIe-5442

Contents

PXIe-5442 Specifications

These specifications apply to the 32 MB, 256 MB, and 512 MB PXIe-5442.

> **Hot Surface** If the PXIe-5442 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PXIe-5442 to cool before removing it from the chassis.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the expected performance met by a majority of the models.
- **Nominal** specifications describe parameters and attributes that may be useful in operation.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Analog filter enabled
- Digital-to-analog converter (DAC) interpolation set to maximum allowed factor for a given sample rate
- Signals terminated with 50 Ω
- Direct path set to 1 V_{pk-pk}, Main path set to 2 V_{pk-pk}
- Sample clock set to 100 MS/s

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature ranges of 0 °C to 55 °C

Typical specifications are valid under the following conditions unless otherwise noted:

- Over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production

CH 0 (Channel 0 Analog Output, Front Panel Connector)

Number of Channels	1
Connector	SMB (jack)

Output Voltage Characteristics

Output paths	The software-selectable Main path provides full-scale voltages from 5.64 $mV_{pk\text{-}pk}$ to 2.00 $V_{pk\text{-}pk}$ into a 50 Ω load. NI-FGEN uses a low-gain amplifier when you select the Main path. The software-selectable Direct path is optimized for intermediate frequency (IF) applications and provides full-scale voltages from 0.707 to 1.000 $V_{pk\text{-}pk}$.
DAC resolution	16 bits

Amplitude and Offset

Table 1. Amplitude Range

Path	Load	Amplitude ($V_{pk\text{-}pk}$)[1]	
		Minimum Value	Maximum Value
Direct	50 Ω	0.707	1.00

Path	Load	Amplitude (V_{pk-pk})[1]	
		Minimum Value	Maximum Value
	1 kΩ	1.35	1.91
	Open	1.41	2.00
Main	50 Ω	0.00564	2.0
	1 kΩ	0.0107	3.81
	Open	0.0113	4.00

Amplitude resolution	<0.06% (0.004 dB) of amplitude range
Offset range	Span of ±25% of amplitude range with increments <0.0014% of amplitude range[2]

Maximum Output Voltage

Table 2. Maximum Output Voltage

Path	Load	Maximum Output Voltage (V_{pk-pk}) [3]
Direct	50 Ω	±0.500
	1 kΩ	±0.953
	Open	±1.000
Main	50 Ω	±1.000
	1 kΩ	±1.905
	Open	±2.000

Accuracy

DC Accuracy[4]

Main ±0.2% of amplitude ± 0.05% of offset ± 500 µV (within ±10 °C of self-calibration temperature)

±0.4% of amplitude ± 0.05% of offset ±1 mV (0 to 55 °C)

Direct	Gain accuracy: ±0.2% (within ±10 °C of self-calibration temperature) Gain accuracy: ±0.4% (0 to 55 °C) DC error: ±30 mV (0 to 55 °C)
AC amplitude accuracy[5]	(+2.0% + 1 mV), (-1.0% - 1 mV) (+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical

Output Characteristics

Output impedance	50 Ω nominal or 75 Ω nominal, software-selectable
Load impedance compensation	Output amplitude is compensated for user-specified load impedances.
Output coupling	DC
Output enable	Software-selectable. When disabled, CH 0 output is terminated with a 1 W resistor with a value equal to the selected output impedance.
Maximum output overload	The CH 0 output terminal can be connected to a 50 Ω, ±12 V (±8 V for the Direct path) source without sustaining any damage. No damage occurs if CH 0 is shorted to ground indefinitely.
Waveform summing	The CH 0 output terminal supports waveform summing among similar paths-specifically, the outputs of multiple PXIe-5442 signal generators can be connected together.

Frequency and Transient Response

Bandwith	>43 MHz, measured at -3 dB

DAC Digital Interpolation Filter[6]	Software-selectable finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.
Analog Filter	Software-selectable 7-pole elliptical filter for image suppression. Available only on Main path

Passband Flatness, with respect to 50 kHz

Direct	-0.4 to +0.6 dB 100 Hz to 40 MHz
Main	-1.0 to +0.5 dB 100 Hz to 20 MHz

Figure 1. Normalized Passband Flatness, Direct Path

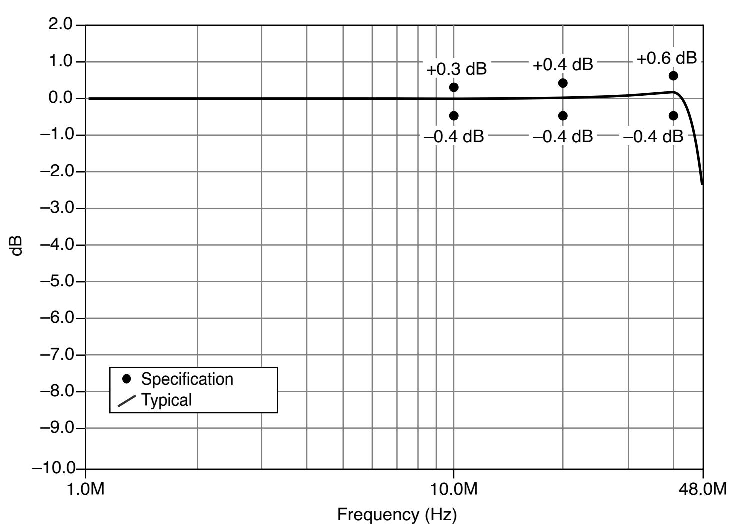
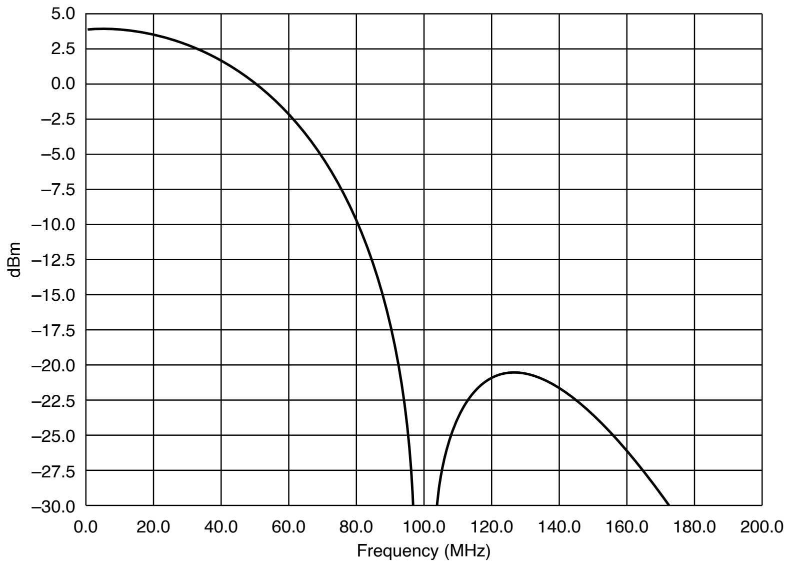


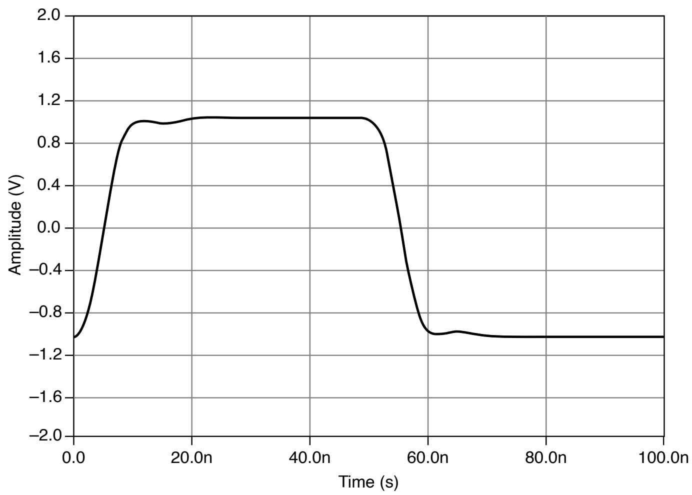
Figure 2. Theoretical Frequency ResponseAbove 50 MHz, the response is the image response. of Direct Path, 100 MS/s, 1x DAC Interpolation, Typical



Pulse Response

Rise/Fall Time (10% to 90%)[7]	
Direct	<5 ns, typical
	<4.5 ns[8], typical
Main	<8 ns, typical
	<5.5 ns[8], typical
Aberration	
Direct	<12%, typical
Main	<5%, typical

Figure 3. Pulse Response, Main Path with 50 Ω Load, Typical



Suggested Maximum Frequencies for Common Functions

Sine	
Direct Path	43 MHz
Main Path	43 MHz
Square	
Direct Path	Not recommended [9]
Main Path	25 MHz
Ramp[10]	
Direct Path	Not recommended[9]
Main Path	5 MHz
Triangle[10]	

Direct Path	Not recommended[9]
Main Path	5 MHz

Spectral Characteristics

Table 3. Spurious-Free Dynamic Range[11] (SFDR) with Harmonics, Typical[12]

Frequency (MHz)	SFDR (dB) with Harmonics, Typical	
	Direct Path	Main Path
1	76	71
10	68	64
20	60	57
30	73	73
40	76	73
43	78	75

Table 4. SFDR without Harmonics, Typical[12]

Frequency (MHz)	SFDR (dB) without Harmonics, Typical	
	Direct Path	Main Path
1	87	90
10	86	88
20	79	88
30	72	72
40	75	72
43	77	74

Table 5. 0 °C to 40 °C Total Harmonic Distortion (THD), Typical [13]

Frequency	THD (dBc), Typical	
	Direct Path	Main Path
20 kHz	-77	-77
1 MHz	-75	-70
5 MHz	-68	-68
10 MHz	-65	-61

Frequency	THD (dBc), Typical	
	Direct Path	Main Path
	-66[14]	-66[14]
20 MHz	-55 -61[14]	-53 -61[14]
30 MHz	-50 -57[14]	-48 -57[14]
40 MHz	-48 -54[14]	-46 -54[14]
43 MHz	-47 -53[14]	-45 -53[14]

Table 6. 0 °C to 55 °C Total Harmonic Distortion (THD) [13]

Frequency	THD (dBc), Typical	
	Direct Path	Main Path
20 kHz	-76	-76
1 MHz	-74	-69
5 MHz	-67	-67
10 MHz	-63	-60
20 MHz	-54 -57[14]	-52 -55[14]
30 MHz	-48 -52[14]	-46 -50[14]
40 MHz	-46 -50[14]	-41 -47[14]
43 MHz	-45 -49[14]	-41 -46[14]

Table 7. Average Noise Density[15], Typical

Path	Amplitude Range		Average Noise Density, Typical		
	$V_{pk\text{-}pk}$	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
Direct	1	4.0	18	-142	-146.0
Main	0.06	-20.4	9	-148	-127.6
	0.1	-16.0	9	-148	-132.0
	0.4	-4.0	13	-145	-141.0
	1	4.0	18	-142	-146.0
	2	10.0	35	-136	-146.0

Figure 4. 10 MHz Single-Tone Spectrum[16], Direct Path, 100 MS/s, 4x DAC Interpolation, Typical

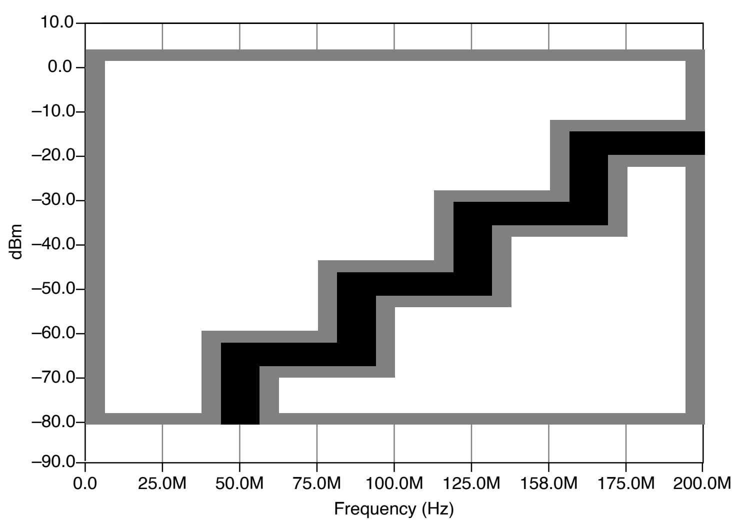


Figure 5. 10 MHz Single-Tone Spectrum[16], Main Path, 100 MS/s, 4x DAC Interpolation, Typical

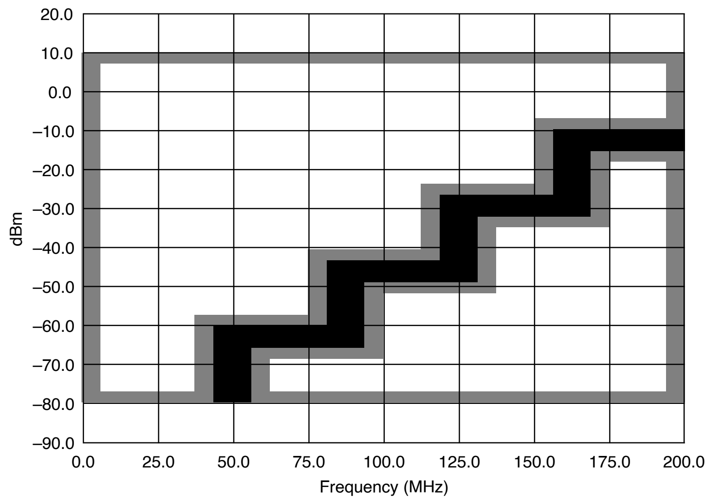
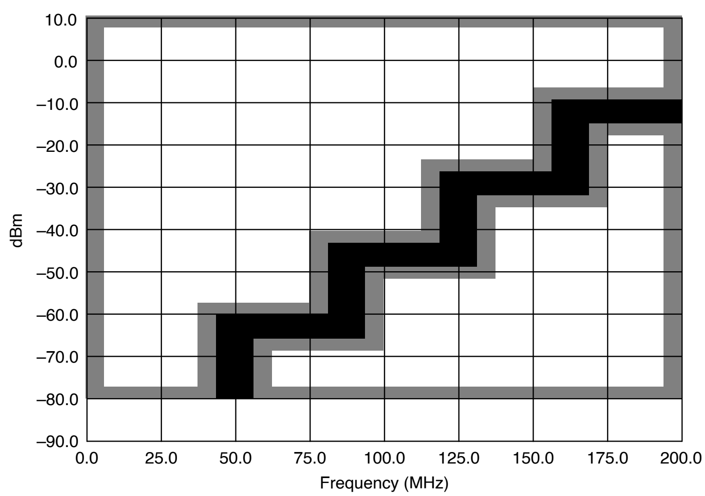


Figure 6. Direct Path, Two-Tone Spectrum[16], Typical



Sample Clock

Sources	Internal, Divide-by-N (N ≥ 1) Internal, DDS-based, High-Resolution External, CLK IN (SMB front panel connector)

	External, PXI star trigger (backplane connector) External, PXI_Trig<0..7> (backplane connector)

Sample Rate Range and Resolution

Sample Clock Source	Sample Rate Range	Sample Rate Resolution
Divide-by-**N**	23.84 S/s to 100 MS/s	Settable to (100 MS/s)/**N** (1 ≤ **N** ≤ 4,194,304)
High Resolution	10 S/s to 100 MS/s	1.06 µHz
CLK IN	200 kS/s to 105 MS/s	Resolution determined by external clock source. External sample clock duty cycle tolerance 40 to 55%.
PXI Star Trigger	10 S/s to 105 MS/s	
PXI_Trig<0..7>	10 S/s to 20 MS/s	

DAC Effective Sample Rate[17]

Sample Rate (MS/s)	DAC Interpolation Factor	Effective Sample Rate
10 S/s to 105 MS/s	1 (off)	10 S/s to 105 MS/s
12.5 MS/s to 105 MS/s	2	25 MS/s to 210 MS/s
10 MS/s to 100 MS/s	4	40 MS/s to 400 MS/s
10 MS/s to 50 MS/s	8	80 MS/s to 400 MS/s

Sample Clock Delay Range and Resolution

Sample Clock Source	Delay Adjustment Range	Delay Adjustment Resolution
Divide-by-**N**	±1 Sample clock period	<10 ps
High-Resolution	±1 Sample clock period	Sample clock period/16,384
External (all)	0 to 7.6 ns	<15 ps

System Phase Noise and Jitter (10 MHz Carrier)

Sample Clock Source	System Phase Noise Density[18] (dBc/Hz) Offset, Typical			System Output Jitter[18], Typical (Integrated from 100 Hz to 100 kHz)
	100 Hz	1 kHz	10 kHz	
Divide-by-**N**	-110	-131	-137	<1.0 ps rms

Sample Clock Source	System Phase Noise Density[18] (dBc/Hz) Offset, Typical			System Output Jitter[18], Typical (Integrated from 100 Hz to 100 kHz)
	100 Hz	1 kHz	10 kHz	
High-Resolution[19]	-114	-126	-126	<4.0 ps rms
CLK IN	-113	-132	-135	<1.1 ps rms
PXI Star Trigger[20]	-115	-118	-130	<3.0 ps rms

External Sample Clock Input Jitter Tolerance

Cycle-cycle jitter	±300 ps, typical
Period Jitter	±1 ns, typical

Sample Clock Exporting

Exported Sample Clock Destinations[21]	Maximum Frequency	Jitter, typical	Duty Cycle
PFI<0..1> (SMB front panel connectors)	105 MHz	PFI 0: 6 ps rms PFI 1: 12 ps rms	25% to 65%
PXI_Trig<0..6> (PXI backplane connector)	20 MHz	—	—

Note Sample clock purity can significantly affect the performance of the PXIe-5442. High amounts of jitter or phase noise in the sample clock can create spurs in the signal generator's spectrum that are not present when using a pure sample clock. For example, if the Clock Mode property is set to Automatic, NI-FGEN often selects High-Resolution clocking to achieve a specific IQ rate. High-Resolution clocking has more jitter than Divide-By-**N** clocking and may create extra spurs in the waveform generator output spectrum. To remove extra spurs without using software resampling, you can use a pure external clock such as the PXI-5650/5651/5652 frequency sources, with low jitter and <1 Hz frequency resolution.

Onboard Clock (Internal VCXO)

Clock Source	Internal Sample clocks can either be locked to a Reference clock using a phase-locked loop or be derived from the onboard voltage-controlled crystal oscillator (VCXO) frequency reference.
Frequency Accuracy	±25 ppm

Phase-Locked Loop (PLL) Reference Clock

Sources[22]	PXI_CLK10 (backplane connector) CLK IN (SMB front panel connector)
Frequency Accuracy	When using the PLL, the frequency accuracy of the PXIe-5442 is solely dependent on the frequency accuracy of the PLL Reference clock source.
Lock Time	
Typical	70 ms
Maximum	200 ms
Frequency Range	5 to 20 MHz in increments of 1 MHz. Default of 10 MHz. The PLL Reference clock frequency must be accurate to ±50 ppm.
Duty Cycle Range	40 to 60%
Exported PLL Reference Clock Destinations	PFI <0..1> (SMB front panel connectors) PXI_Trig<0..6> (backplane connector)

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Connector	SMB (jack)
Direction	Input
Destinations	Sample clock PLL Reference clock
Frequency Range	1 MHz to 105 MHz (Sample clock destination and sine waves) 200 kHz to 105 MHz (Sample clock destination and square waves) 5 MHz to 20 MHz (PLL Reference clock destination)
Input Voltage Range	
Sine wave	0.65 $V_{pk\text{-}pk}$ to 2.8 $V_{pk\text{-}pk}$ into 50 Ω (0 dBm to +13 dBm)
Square wave	0.2 $V_{pk\text{-}pk}$ to 2.8 $V_{pk\text{-}pk}$ into 50 Ω
Maximum Input Overload	±10 V
Input Impedance	50 Ω
Input Coupling	AC

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Connectors	Two SMB (jacks)

Direction	Bidirectional
Frequency Range	DC to 105 MHz

As an Input (Trigger)

Destinations	Start trigger, Script trigger
Maximum Input Overload	-2 V to +7 V
V_{IH}	2.0 V
V_{IL}	0.8 V
Input Impedance	1 kΩ

As an Output (Event)

Sources	Sample clock divided by integer K (1 ≤ K ≤ 4,194,304) Sample clock timebase (100 MHz) divided by integer M (2 ≤ M ≤ 4,194,304) PLL Reference clock Marker event Data Marker event Exported Start trigger Exported Script trigger

	Ready for Start event Started event Done event
Output Impedance	50 Ω
Maximum Output Overload	-2 V to +7 V
V_{OH}[23]	Minimum: 2.9 (open load), 1.4 V (50 Ω load)
V_{OL}[23]	Maximum: 0.2 (open load), 0.2 V (50 Ω load)
Rise/Fall Time	≤2.0 ns (load of 10 pF)

Start Trigger

Sources	PFI <0..1> (SMB front panel connectors) PXI_Trig<0..7> (backplane connector) Software, can be configured through NI-FGEN programming calls Immediate (does not wait for a trigger). Default value for the Start trigger source
Modes	Single Continuous Stepped

	Burst
Edge Detection	Rising
Minimum Pulse Width	25 ns

Table 8. Delay from Start Trigger to CH 0 Analog Output with OSP Disabled

DAC Interpolation Factor	Delay, Typical
Digital Interpolation Filter disabled	46 Sample clock periods + 110 ns
2	60 Sample clock periods + 110 ns
4	66 Sample clock periods + 110 ns
8	67 Sample clock periods + 110 ns

Additional Delay for Function Generator Mode	Add 37 Sample clock periods, applicable to delay from Start trigger to CH 0 analog output.
Additional Delay with OSP Enabled[24]	(29 to 120 Sample clock periods) + (0 to 40 IQ clock periods), applicable to delay from Start trigger to CH 0 analog output.
Additional Delay for Function Generator Mode	Add 37 Sample clock periods, applicable to delay from Start trigger to CH 0 analog output.
Additional Delay with OSP Enabled[25]	(29 to 120 Sample clock periods) + (0 to 40 IQ clock periods), applicable to delay from Start trigger to CH 0 analog output.

Trigger Exporting

Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the Destinations specification of the Markers section.
Exported Trigger Delay	65 ns, typical
Exported Trigger Pulse Width	>150 ns

Markers

Destinations	PFI <0..1> (SMB front panel connectors) PXI_Trig<0..6> (backplane connector)
Quantity	One marker per segment
Quantum	Marker position must be placed at an integer multiple of one sample.
Width	>150 ns
Skew	
PFI<0..1>	±2 Sample clock periods
PXI_Trig<0..6>	±2 Sample clock periods
Jitter, typical	20 ps rms

Arbitrary Waveform Generation Mode

Memory usage	The PXIe-5442 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.
Onboard memory size	
32 MB	33,554,432 bytes
256 MB	268,435,456 bytes

512 MB	536,870,912 bytes

Output modes

Arbitrary Waveform	A single waveform is selected from the set of waveforms stored in onboard memory and generated.
Arbitrary Sequence	A sequence directs the PXIe-5442 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.

Table 9. Minimum Waveform Size (Samples)[26]

Trigger Mode	Arbitrary Waveform Mode	Arbitrary Sequence Mode
Single	16	16
Continuous	16	96 @ > 50 MS/s
		32 @ ≤ 50 MS/s
Stepped	32	96 @ > 50 MS/s
		32 @ ≤ 50 MS/s
Burst	16	512 @ >50 MS/s
		256 @ ≤ 50 MS/s

Loop count	1 to 16,777,215 Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of one sample of either real or complex (IQ) data

Table 10. Memory Limits (in Samples)[27]

	32 MB	256 MB	512 MB
Arbitrary Waveform Mode, Maximum Waveform Memory [28]	16,777,088	134,217,600	268,435,328

	32 MB	256 MB	512 MB
Arbitrary Sequence Mode, Maximum Waveform Memory[28] [29] ,	16,777,008	134,217,520	268,435,200
Arbitrary Sequence Mode, Maximum Waveforms [30]	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	4,194,000 Burst trigger: 524,000
Arbitrary Sequence Mode, Maximum Segments in a Sequence [31]	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	6,708,000 Burst trigger: 4,180,000

Table 11. Waveform Play Times [32]

	32 MB	256 MB	512 MB
Maximum Play Time, Sample Rate = 100 MS/s, OSP Disabled	0.16 seconds	1.34 seconds	2.68 seconds
Maximum Play Time, IQ Rate = 1 MS/s, Real Mode, OSP Enabled	16 seconds	2 minutes and 14 seconds	4 minutes and 28 seconds
Maximum Play Time, IQ Rate = 100 kS/s, Real Mode, OSP Enabled	2 minutes and 47 seconds	22 minutes and 22 seconds	44 minutes and 43 seconds

Function Generation Mode

Standard Waveforms and Maximum Frequencies[33]

Sine	43 MHz
Square	25 MHz
Triangle	5 MHz
Ramp Up	5 MHz
Ramp Down	5 MHz

DC	—
Noise (pseudorandom)	5 MHz
User Defined	43 MHz

Memory Size (in Samples)[34]	131,072 for 1/4 symmetric waveforms (Example: sine) 32,768 for non-1/4 symmetric waveforms (Example: ramp)
Frequency Resolution	355 nHz
Phase Resolution	0.0055°

Onboard Signal Processing (OSP)

IQ Rate

OSP Interpolation Range[35]	1, 2, 4, 6, 8, 10 12 to 4,096 (multiples of 4) 4,096 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16)
IQ Rate[36]	Sample rate/OSP interpolation (Lower IQ rates are possible by either lowering the sample rate or doing software interpolation)

Bandwidth[37]

Real Flat	0.4 x IQ Rate

Complex Flat	0.8 x IQ Rate
Data Processing Modes	Real (I path only) Complex IQ

Prefilter Gain and Offset

Prefilter Gain and Offset Resolution	18 bits
Prefilter Gain Range[38]	-2.0 to +2.0 (|Values| < 1 attenuate user data)
Prefilter Offset Range[39]	-1.0 to +1.0
Output[40]	(User data x Prefilter gain) + Prefilter offset(-1 ≤ output ≤ +1)

Table 12. Finite Impulse Response (FIR) Filter Types

Type	Parameter	Minimum	Maximum
Flat[41]	Passband	0.4	0.4
Raised Cosine[42]	Alpha	0.1	0.4
Root Raised Cosine[42]	Alpha	0.1	0.4

Numerically Controlled Oscillator (NCO)

Frequency Range	1 mHz to (0.43 x sample rate)
Frequency Resolution[43]	Sample rate / 2^{48}

I and Q Phase Resolution	0.0055°
Phase Quantization[44]	17 bits
Tuning Speed	1 ms

Table 13. IF Modulation Performance, Typical [45]

Modulation Configuration	Measurement Type	Value
GSM Physical Layer[46]	MER (Modulation Error Ratio)	56 dB
	EVM (Error Vector Magnitude)	<0.2% rms
W-CDMA Physical Layer[47]	MER	48 dB
	EVM	<0.4% rms
DVB Physical Layer[48]	MER	44 dB
	EVM	<0.5% rms
20 MSymbols/s 64 QAM[49]	MER	39 dB
	EVM	<0.8% rms
26.09 MSymbols/s 64 QAM[49]	MER	36 dB
	EVM	<1.0% rms
34.78 MSymbols/s 64 QAM[49]	MER	32 dB
	EVM	<1.6% rms

Digital Performance

Maximum NCO Spur[50]	<-90 dBc
Interpolating Flat Filter Passband Ripple[51]	<0.1 dB
Interpolating Flat Filter out of Band Suppression[52]	>80 dB

Figure 7. Real Interpolation Filter Frequency Response IQ Rate = 10 MS/s

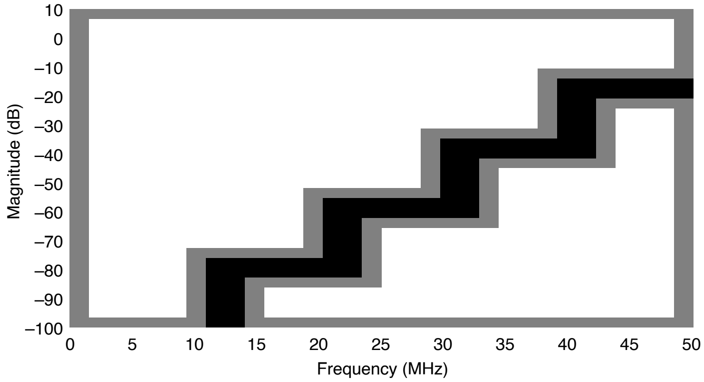


Figure 8. GSM Physical Layer[53] External Sample Clocking = 99.665 MHz

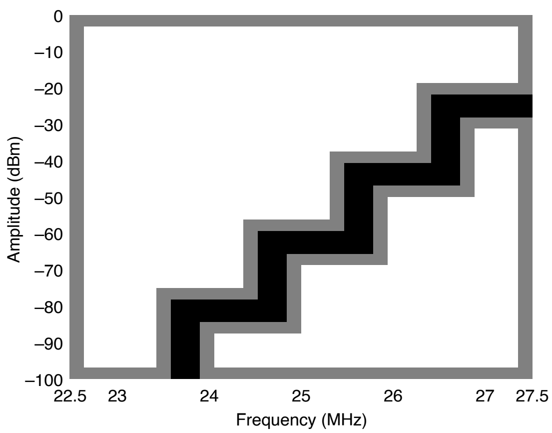


Figure 9. GSM Physical Layer[53][54] Internal (High-Resolution) Sample Clocking = 99.665 MHz

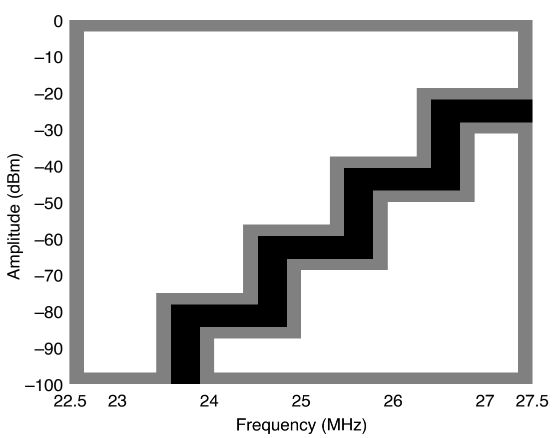


Figure 10. DVB Physical Layer[55] External Sample Clocking = 96.88 MHz

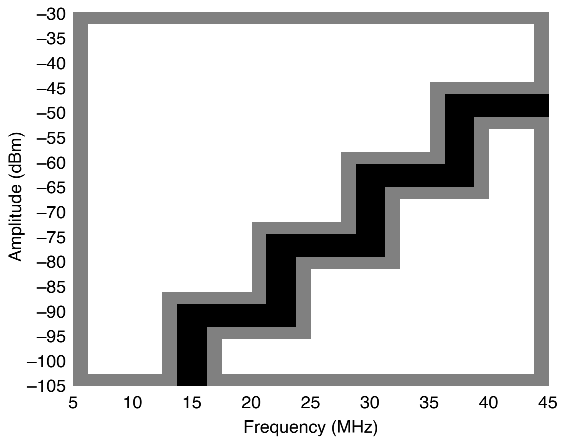


Figure 11. DVB Physical Layer[55][54] Internal (High-Resolution) Sample Clocking = 96.88 MHz

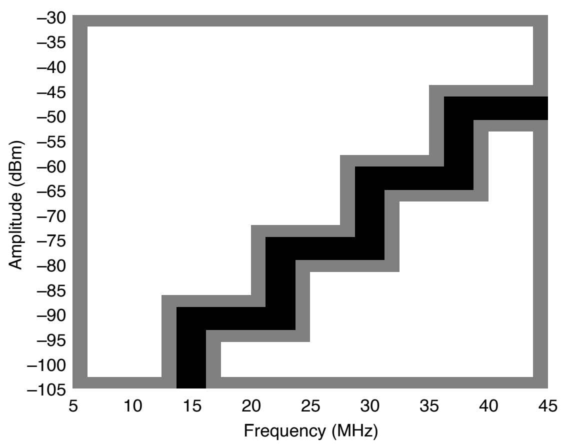


Figure 12. W-CDMA Physical Layer[56] Internal (High-Resolution) Sample Clocking = 92.16 MHz

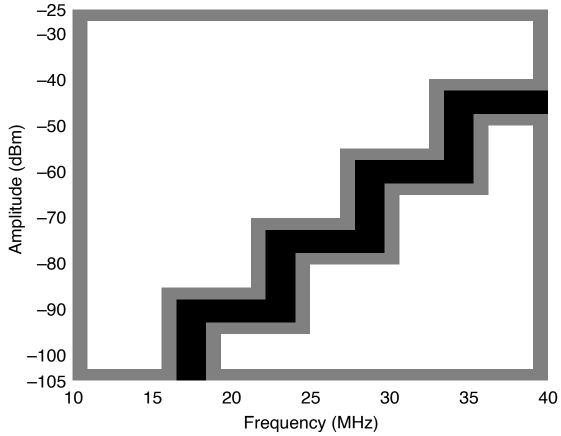
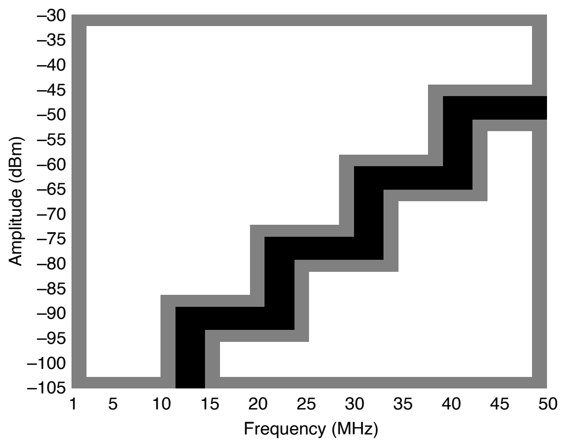


Figure 13. 20 MSymbols/s 64 QAM[57]



Calibration

Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.
External Calibration	The external calibration calibrates the VCXO, voltage reference, output impedance, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.

Calibration Interval	Specifications valid within 2 years of external calibration
Warm-up Time	15 minutes

Power

+3.3 VDC	1.67 A, typical 2.0 A, maximum
+12 VDC	1.9 A, typical 2.2 A, maximum
Total power	28.3 W, typical 33 W, maximum

Physical Characteristics

Dimensions	3U, one-slot, PXI Express module 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)
Weight	405 g (14.3 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-25 °C to 85 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the Online Product Certification section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

> **Note** For EMC declarations and certifications, refer to the Online Product Certification section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Minimize Our Environmental Impact** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

> **EU Customers** At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more

information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

1 Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, you can use waveforms less than the full scale of the DAC. NI-FGEN compensates for user-specified resistive loads.

2 Not available on the Direct path

3 The maximum output voltage of the PXIe-5442 is determined by the amplitude range and the offset range

4 All paths are calibrated for amplitude and gain errors. The Main path is also calibrated for offset errors.

5 50 kHz sine wave. Signals terminated with high impedance

6 Refer to the Onboard Signal Processing (OSP) section for OSP Interpolation information.

7 Analog filter and DAC interpolation filter disabled.

8 Specifications apply only to B-revision and later PXIe-5442 devices (National Instruments part number 196749B-0XL).

9 Direct Path is optimized for the frequency domain

10 Disable the analog filter and the DAC interpolation filter.

[11] Dynamic range is defined as the difference between the carrier level and the largest spur .

[12] Amplitude -1 dBFS. Measured from DC to 50 MHz. All values include aliased harmonics.

[13] Amplitude -1 dBFS. Includes the 2nd through the 6th harmonic.

[14] Specifications apply only to B-revision and later PXIe-5442 devices (National Instruments part number 196749B-0XL).

[15] Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor.

[16] The noise floor is limited by the measurement device. Refer to the Average Noise Density specifications for more information about this limit.

[17] DAC Effective Sample Rate = (DAC Interpolation factor) * (Sample Rate). Refer to the Onboard Signal Processing (OSP) section for OSP interpolation information.

[18] Specified at 2x DAC oversampling.

[19] High-Resolution specifications increase as the sample rate is decreased .

[20] PXI star trigger specification is valid when the sample clock source is locked to PXI_CLK10.

[21] Exported sample clocks can be divided by integer **K** (1 ≤ **K** ≤ 4,194,304).

[22] The PLL Reference clock provides the reference frequency for the PLL

[23] Output drivers are +3.3 V TTL compatible.

[24] Varies with OSP configuration

[25] Varies with OSP configuration

[26] The minimum waveform size is sample rate dependent in Arbitrary Sequence mode. For complex (IQ) data, minimum waveform size is halved.

[27] All trigger modes except where noted.

[28] For IQ data, maximum waveform memory is halved.

[29] Condition: One or two segments in a sequence

[30] Condition: One or two segments in a sequence

[31] Condition: Waveform memory is <4,000 (<2,000 for IQ data).

[32] Single trigger mode. Play times can be significantly extended by using Continuous, Stepped, or Burst trigger modes. For IQ mode the play times are halved.

[33] Minimum frequency is 0 Hz for all waveforms.

[34] 16-bit samples. User-defined waveforms must be exactly 32,768 samples

[35] Total PXIe-5442 interpolation = OSP interpolation x DAC interpolation

[36] Example: For a Sample rate of 100 MS/s, IQ rate range = 6.1 kS/s to 100 MS/s

[37] Example: Complex bandwidth is 40 MHz with a complex IQ rate of 50 MS/s

[38] Unitless

[39] Applied after Prefilter gain

[40] Prefilter output

[41] Lowpass filter that minimizes ripple to IQ rate x Passband.

[42] These filters can only be used with an OSP interpolation factor of 12 or greater

[43] Example: 355 nHz with a sample rate of 100 MS/s

[44] Look-up table address width

45 Direct path (4 dBm peak), 25 MHz carrier

46 OSP Enabled. IQ Rate = 1.083 MS/s, 4 Samples/Symbol. FIR Filter Type = Flat, Passband = 0.4, Prefilter Gain = 0.4. MSK modulation. Software Pulse Shaping and Phase Accumulation, 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 11.

47 OSP Enabled. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.22, Prefilter Gain = 0.35. QPSK modulation. PN Sequence Order = 12.

48 OSP Enabled. IQ Rate = 6.92 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.15, Prefilter Gain = 0.4. 32 QAM modulation. PN Sequence Order = 12

49 OSP Enabled. IQ Rate = 50 MS/s. FIR Filter Type = Flat, Passband=0.4, Prefilter Gain = 0.6. 64 QAM modulation. Software Pulse Shaping and Resampling, Root-Raised Cosine, Alpha = 0.15. PN Sequence Order = 15.

50 Full-scale output

51 Passband from 0 to (0.4 x IQ rate)

52 Stopband suppression from (0.6 x IQ rate)

53 OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 1.083 MS/s, 4 samples/symbol. FIR Filter Type = Flat, Passband = 0.4. Software MSK modulation: 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 14. For more information about eliminating spurs, refer to the Sample Clock section.

54 Additional Artifacts are due to High-Resolution Clock Spurs.

55 OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 6.92 MS/s, 1 sample/symbol. FIR Filter Type = Root- Raised Cosine, Alpha = 0.15. 32 QAM modulation. PN Sequence Order = 15. For more information about eliminating spurs, refer to the Sample Clock section.

[56] OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.22. QPSK modulation. PN Sequence Order = 15.

[57] OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 50 MHz. FIR Filter Type = Flat Passband = 0.4. Software 64 QAM modulation. Root-Raised Cosine Alpha = 0.15. PN Sequence Order = 15.