PCI/PXI-6280 Specifications

Contents

NI 6280 Specifications

Analog Input

Number of channels	8 differential or 16 single ended
ADC resolution	18 bits
DNL	No missing codes guaranteed
INL	Refer to the AI Absolute Accuracy section
Sample rate Single channel maximum Multichannel maximum (aggregate) Minimum	 625 kS/s 500 kS/s No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Input coupling	DC
Input range	±0.1 V, ±0.2 V, ±0.5 V, ±1 V, ±2 V, ±5 V, ±10 V
Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND

CMRR (DC to 60 Hz)	110 dB
Input impedance **Device on** AI+ to AI GND AI- to AI GND **Device off** AI+ to AI GND AI- to AI GND	>10 GΩ in parallel with 100 pF >10 GΩ in parallel with 100 pF 820 Ω 820 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz) Adjacent channels Non-adjacent channels	 -75 dB -95 dB
Small signal bandwidth (-3 dB)	750 kHz filter off, 40 kHz filter on
Input FIFO size	2,047 samples
Scan list memory	4,095 entries
Data transfers	DMA (scatter-gather), interrupts, programmed I/O
Overvoltage protection for all analog input and sense channels Device on	 ±25 V for up to eight AI pins

Device off	±15 V for up to eight AI pins
Input current during overvoltage condition	±20 mA maximum/AI pin

Table 1. Settling Time for Multichannel Measurements

Range	Filter Off ±15 ppm of Step (±4 LSB for Full-Scale Step)	Filter Off ±4 ppm of Step (±1 LSB for Full-Scale Step)	Filter On ±4 ppm of Step (±1 LSB for Full-Scale Step)
±5 V, ±10 V	2 µs	8 µs	50 µs
±0.5 V, ±1 V, ±2 V	2.5 µs	8 µs	50 µs
±0.1 V, ±0.2 V	3 µs	8 µs	50 µs

Typical Performance Graphs

Figure 1. AI Settling Error versus Time for Different Source Impedances

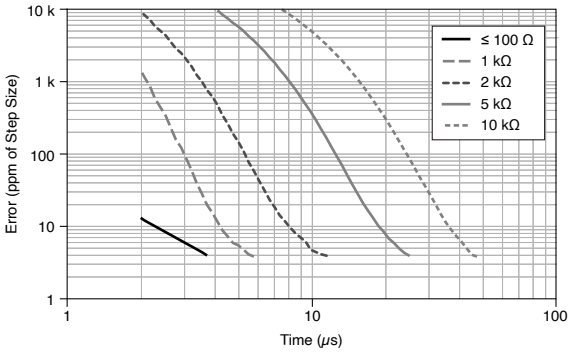


Figure 2. AI Small Signal Bandwidth

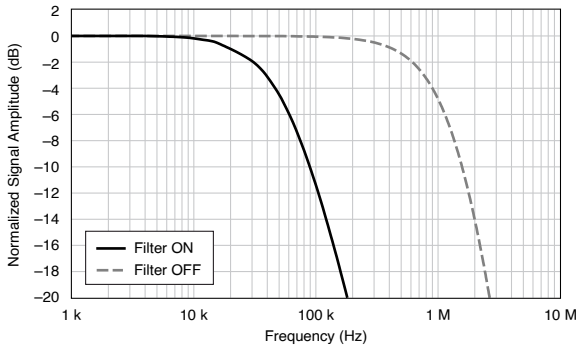
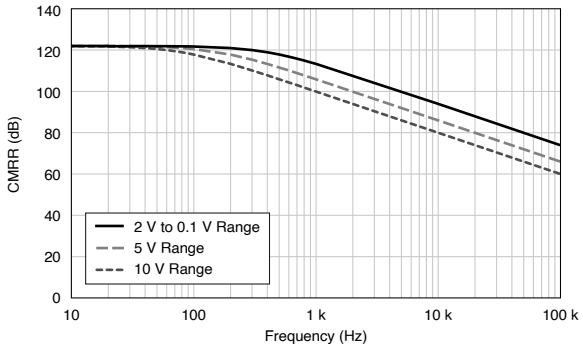


Figure 3. AI CMRR



AI Absolute Accuracy

AI Absolute Accuracy (Filter On)

Note Accuracies listed are valid for up to two years from the device external calibration.

Table 4. AI Absolute Accuracy (Filter On)

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)	Sensitivity (µV)
10	-10	40	8	11	60	980	24
5	-5	45	8	11	30	510	12
2	-2	45	8	13	12	210	4.8
1	-1	55	15	15	7	120	2.8
0.5	-0.5	55	30	20	4	70	1.6
0.2	-0.2	75	45	35	3	39	1.2
0.1	-0.1	120	60	60	2	28	0.8

Note Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Gain tempco	17 ppm/°C
Reference tempco	1 ppm/°C
INL error	10 ppm of range

AI Absolute Accuracy (Filter Off)

Note Accuracies listed are valid for up to two years from the device external calibration.

Table 4. AI Absolute Accuracy (Filter Off)

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)	Sensitivity (µV)
10	-10	45	10	11	70	1,050	28.0

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)	Sensitivity (µV)
5	-5	50	10	11	35	550	14.0
2	-2	50	10	13	15	230	6.0
1	-1	60	17	15	12	130	4.8
0.5	-0.5	60	32	20	10	80	4.0
0.2	-0.2	80	47	35	9	43	3.6
0.1	-0.1	120	62	60	9	31	3.6

Note Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Gain tempco	17 ppm/°C
Reference tempco	1 ppm/°C
INL error	10 ppm of range

AI Absolute Accuracy Equation

AbsoluteAccuracy = **Reading** · **(GainError)** + **Range** · **(OffsetError)** + **NoiseUncertainty**

- **GainError** = **ResidualAIGainError** + **GainTempco** · **(TempChangeFromLastInternalCal)** + **ReferenceTempco** · **(TempChangeFromLastExternalCal)**
- **OffsetError** = **ResidualAIOffsetError** + **OffsetTempco** · **(TempChangeFromLastInternalCal)** + **INLError**
- **NoiseUncertainty** = $\frac{\text{Random Noise} \quad 3}{\sqrt{100}}$ for a coverage factor of 3 σ and averaging 100 points.

AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- TempChangeFromLastExternalCal = 10 °C
- TempChangeFromLastInternalCal = 1 °C
- number_of_readings = 100
- CoverageFactor = 3 σ

For example, on the 10 V range of the Filter On accuracy table, the absolute accuracy at full scale is as follows:

- GainError = 40 ppm + 17 ppm · 1 + 1 ppm · 10 = 67 ppm
- OffsetError = 8 ppm + 11 ppm · 1 + 10 ppm = 29 ppm
- NoiseUncertainty = $\frac{60\ \mu V\ 3}{\sqrt{100}}$ = 18 µV
- AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty = 980 µV

Analog Triggers

Number of triggers	1
Source	AI <0..15>, APFI 0
Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Source level	
AI <0..15>	±Full scale

APFI 0	±10 V
Resolution	10 bits, 1 in 1,024
Modes	Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering
Bandwidth (-3 dB)	
AI <0..15>	700 kHz filter off, 40 kHz filter on
APFI 0	5 MHz
Accuracy	±1%
APFI 0 characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection, power on	±30 V
Protection, power off	±15 V

Digital I/O/PFI

Static Characteristics

Number of channels	24 total, 8 (P0.<0..7>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
I/O type	5 V TTL/CMOS compatible

Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection	±20 V on up to two pins[1]

Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..7>)
Port/sample size	Up to 8 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	2,047 samples
DI Sample Clock frequency	0 MHz to 10 MHz, system and bus activity dependent
DO Sample Clock frequency	
Regenerate from FIFO	0 MHz to 10 MHz
Streaming from memory	0 MHz to 10 MHz, system and bus activity dependent
Data transfers	DMA (scatter-gather), interrupts, programmed I/O
DI or DO Sample Clock source[2]	Any PFI, RTSI, AI Sample or Convert Clock, Ctr **n** Internal Output, and many other signals

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, counter, DI, DO timing signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Recommended Operating Conditions

Level	Minimum	Maximum
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH}) P0.<0..7>	—	-24 mA
Output high current (I_{OH}) PFI <0..15>/P1/P2	—	-16 mA
Output low current (I_{OL}) P0.<0..7>	—	24 mA
Output low current (I_{OL}) PFI <0..15>/P1/P2	—	16 mA

Electrical Characteristics

Level	Minimum	Maximum
Positive-going threshold (VT+)	—	2.2 V
Negative-going threshold (VT-)	0.8 V	—
Delta VT hystersis (VT+ - VT-)	0.2 V	—
I_{IL} input low current (V_{in} = 0 V)	—	-10 µA
I_{IH} input high current (V_{in} = 5 V)	—	250 µA

Digital I/O Characteristics

Figure 4. Digital I/O (P0.<0..7>): I_{oh} versus V_{oh}

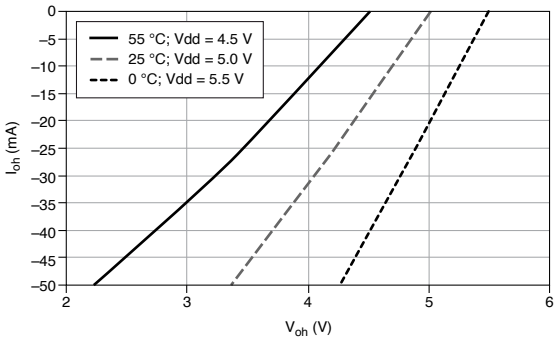


Figure 5. Digital I/O (PFI <0..15>/P1/P2): I_{oh} versus V_{oh}

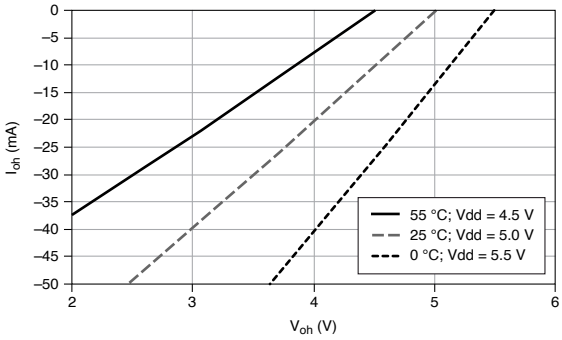


Figure 6. Digital I/O (P0.<0..7>): I_{ol} versus V_{ol}

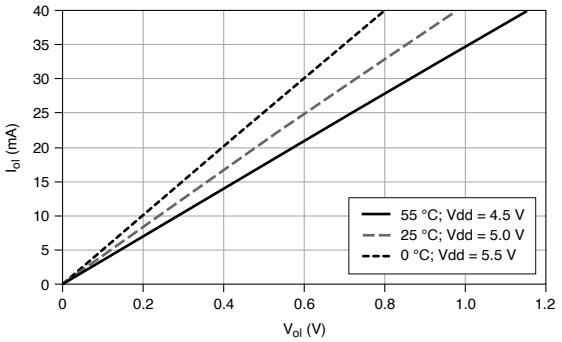
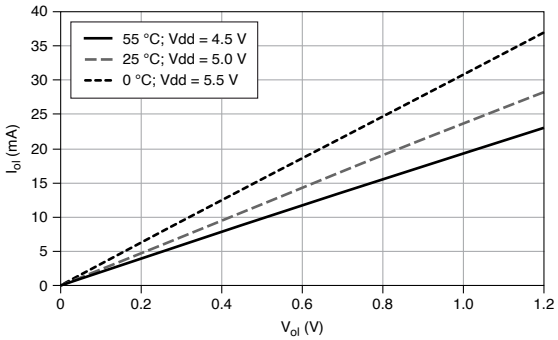


Figure 7. Digital I/O (PFI <0..15>/P1/P2): I_{ol} versus V_{ol}



General-Purpose Counters/Timers

Number of counter/timers	2
Resolution	32 bits
Counter measurements	Edge counting, pulse, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	80 MHz, 20 MHz, 0.1 MHz
External base clock frequency	0 MHz to 20 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down

Routing options for inputs	Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
FIFO	2 samples
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer; interrupts; programmed I/O

Frequency Generator

Number of channels	1
Base clocks	10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm

Output can be available on any output PFI or RTSI terminal.

Phase-Locked Loop (PLL)

Number of PLLs	1
Reference signal	PXI_STAR, PXI_CLK10, RTSI <0..7>
Output of PLL	80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Counter/timer function	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Digital waveform generation (DO) function	Sample Clock
Digital waveform acquisition (DI) function	Sample Clock

Device-to-Device Trigger Bus

PCI	RTSI <0..7>[3]
PXI	PXI_TRIG <0..7>, PXI_STAR
Output selections	10 MHz Clock, frequency generator output, many internal signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Bus Interface

PCI/PXI	3.3 V or 5 V signal environment

DMA channels	6, can be used for analog input, digital input, digital output, counter/timer 0, counter/timer 1

The PXI device supports one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

Table 4. PXI/SCXI Combo and PXI Express Chassis Compatibility

M Series Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
191501C-04	No	Yes
191501A-0**x**/191501B-0**x**	Yes	No

Power Requirements

Current draw from bus during no-load condition[4]	
+5 V	0.03 A
+3.3 V	0.78 A
+12 V	0.40 A
-12 V	0.06 A
Current draw from bus during AI overvoltage condition[4]	
+5 V	0.03 A
+3.3 V	1.26 A
+12 V	0.43 A
-12 V	0.06 A

Current Limits

Caution Exceeding the current limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI, +5 V terminal	1 A maximum[5]
PXI	
+5 V terminal	1 A maximum[5]
P0/PFI/P1/P2 and +5 V terminals combined	2 A maximum

Physical Characteristics

Dimensions	
PCI printed circuit board	10.6 cm × 15.5 cm(4.2 in. × 6.1 in.)
PXI printed circuit board	Standard 3U PXI

Weight	
PCI	151 g (5.3 oz)
PXI	218 g (7.7 oz)

Calibration

Recommended warm-up time	15 minutes
Calibration interval	2 years

Maximum Working Voltage

Connect only voltages that are below these limits.

Channel-to-earth	11 V, Measurement Category I

Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.

Caution Do not use for measurements within Categories II, III, or IV.

Note Measurement Categories CAT I and CAT O (Other) are equivalent. These test and measurement circuits are not intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

Environmental

Operating temperature	0 °C to 55 °C
Storage temperature	-20 °C to 70 °C
Humidity	10% RH to 90% RH, noncondensing
Maximum altitude	2,000 m
Pollution Degree (indoor use only)	2

Indoor use only.

Shock and Vibration (PXI Only)

Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

CE Compliance CE

- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

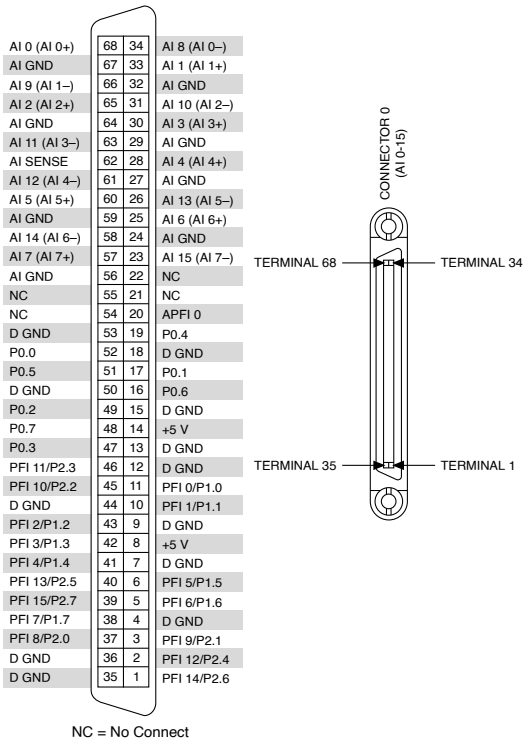
- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Device Pinout

Figure 8. NI PCI/PXI-6280 Pinout



[1] Stresses beyond those listed under **Input voltage protection** may cause permanent damage to the device.

[2] The digital subsystem does not have its own dedicated internal timing engine. Therefore, a sample clock must be provided from another subsystem on the device or an external source.

[3] In other sections of this document, RTSI refers to RTSI <0..7> for the PCI devices or PXI_TRIG <0..7> for PXI devices.

[4] Does not include P0/PFI/P1/P2 and +5 V terminals.

[5] Older revisions have a self-resetting fuse that opens when current exceeds this specification. Newer revisions have a traditional fuse that opens when current exceeds this specification. This fuse is not customer-replaceable; if the fuse permanently opens, return the device to NI for repair.