PXI-5441 Specifications

Contents

PXI-5441 Specifications

These specifications apply to the 32 MB, 256 MB, and 512 MBPXI-5441.

> **Notice** To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Analog filter enabled
- Digital-to-analog converter (DAC) interpolation set to maximum allowed factor for a given sample rate
- Signals terminated with 50 Ω
- Direct path set to 1 V_{pk-pk}, Low-Gain Amplifier path set to 2 V_{pk-pk}, and High-Gain Amplifier path set to 12 V_{pk-pk}

- Sample clock set to 100 MS/s

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature ranges of 0 °C to 55 °C

Typical specifications are valid under the following conditions unless otherwise noted:

- Over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production

CH 0

(Channel 0 Analog Output, Front Panel Connector)

Number of channels	1
Connector	SMB (jack)

Output Voltage Characteristics

Output paths	The software-selectable Main Output path setting provides full-scale voltages from 12.00 $V_{pk\text{-}pk}$ to 5.64 $mV_{pk\text{-}pk}$ into a 50 Ω load. NI-FGEN uses either the Low-Gain Amplifier or the High-Gain Amplifier when the Main Output path is selected, depending on the Gain attribute. The software-selectable Direct path is optimized for intermediate frequency (IF) applications and provides full-scale voltages from 0.707 to 1.000 $V_{pk\text{-}pk}$.
DAC resolution	16 bits

Amplitude and Offset

Table 2. Amplitude Range[1]

Path	Load	Minimum Amplitude Value (V_{pk-pk})	Maximum Amplitude Value (V_{pk-pk})
Direct	50 Ω	0.707	1.00
	1 kΩ	1.35	1.91
	Open	1.41	2.00
Low-Gain Amplifier	50 Ω	0.00564	2.00
	1 kΩ	0.0107	3.81
	Open	0.0113	4.00
High-Gain Amplifier	50 Ω	0.0338	12.0
	1 kΩ	0.0644	22.9
	Open	0.0676	24.0

Amplitude resolution	<0.06% (0.004 dB) of amplitude range
Offset range	Span of ±25% of the amplitude range with increments <0.0014% of amplitude range[2]

Maximum Output Voltage

Table 2. Maximum Output Voltage[3]

Path	Load	Maximum Output Voltage (V_{pk-pk})
Direct	50 Ω	±0.500
	1 kΩ	±0.953
	Open	±1.000
Low-Gain Amplifier	50 Ω	±1.000
	1 kΩ	±1.905
	Open	±2.000
High-Gain Amplifier	50 Ω	±6.000
	1 kΩ	±11.43
	Open	±12.00

Accuracy

DC Accuracy[4]	
Low-Gain or High-Gain Amplifier path	±0.2% of amplitude range ±0.05% of offset ±500 µV (within ±10 °C of self-calibration temperature) ±0.4% of amplitude range ±0.05% of offset ±1 mV (0 to 55 °C)
Direct path	Gain accuracy: ±0.2% amplitude range (within ±10 °C of self-calibration temperature) Gain accuracy: ±0.4% amplitude range (0 to 55 °C) DC error: ±30 mV (0 to 55 °C)
AC amplitude accuracy[5]	(+2.0% + 1 mV), (-1.0% - 1 mV) (+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical

Output Characteristics

Output impedance	50 Ω nominal or 75 Ω nominal, software-selectable
Load impedance compensation	Output amplitude is compensated for user-specified load impedances.
Output coupling	DC
Output enable	Software-selectable. When disabled, CH 0 output is terminated with a 1 W resistor with a value equal to the selected output impedance

Maximum output overload	The CH 0 output terminal can be connected to a 50 Ω, ±12 V (±8 V for the Direct path) source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.
Waveform summing	The CH 0 output supports waveform summing among similar paths-specifically, the output terminals of multiple PXI-5441 signal generators can be connected together.

Frequency and Transient Response

Bandwidth[6]	43 MHz
DAC digital interpolation filter[7]	Software-selectable finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.
Analog filter[8]	Software-selectable 7-pole elliptical filter for image suppression.

Passband flatness[9]

Direct path	-0.4 to +0.6 dB (100 Hz to 40 MHz)
Low-gain amplifier path	-1.0 to +0.5 dB (100 Hz to 20 MHz)
High-gain amplifier path	-1.2 to +0.5 dB (100 Hz to 20 MHz)

Pulse response[10]

Rise/fall time

Direct path	<5 ns
	<4.5 ns, typical[11]
Low-gain amplifier path	<8 ns

	<7 ns[11]
	<5.5 ns, typical[11]
High-gain amplifier path	<10 ns
Aberration	
Direct path	<10%, typical
Low-gain amplifier path	<5%, typical
High-gain amplifier path	<5%, typical

Figure 1. Normalized Passband Flatness, Direct Path

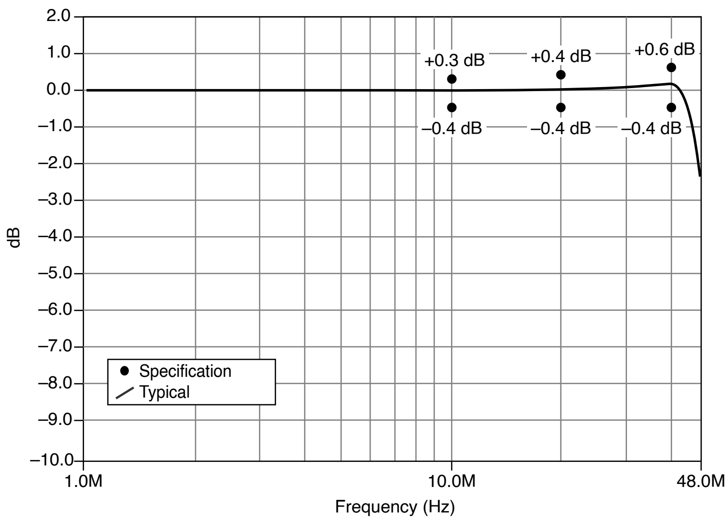


Figure 2. Pulse Response, Low-Gain Amplifier Path 50 Ω Load

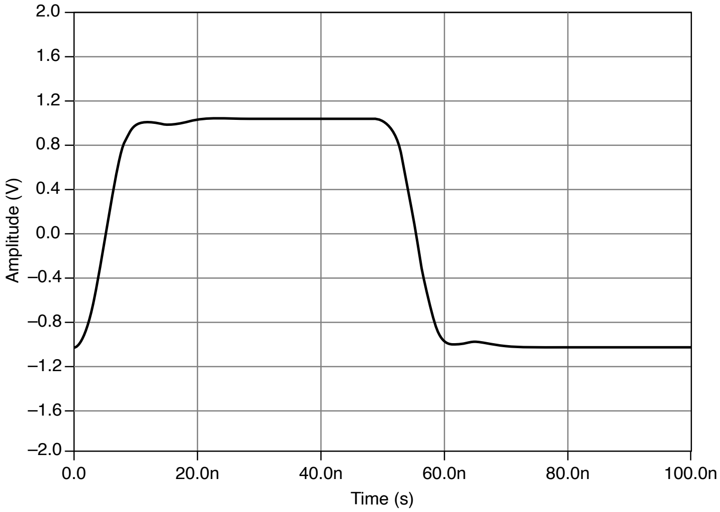
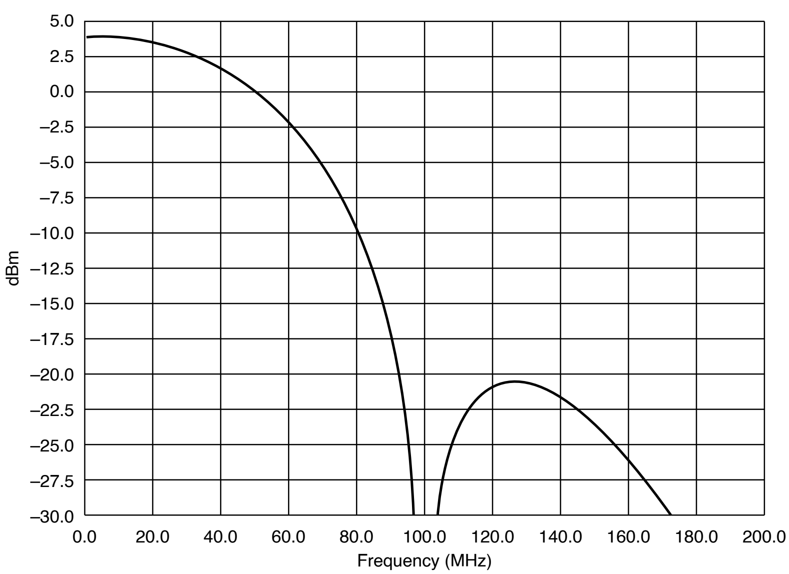


Figure 3. Frequency Response of Direct Path, 100 MS/s, 1x DAC Interpolation[12]



Suggested Maximum Frequencies for Common Functions[13]

Direct	
Sine	43 MHz

Square	Not recommended[14]
Ramp	Not recommended[14]
Triangle	Not recommended[14]
Low-Gain Amplifier	
Sine	43 MHz
Square	25 MHz
Ramp	5 MHz
Triangle	5 MHz
High-Gain Amplifier	
Sine	43 MHz
Square	12.5 MHz
Ramp	5 MHz
Triangle	5 MHz

Spectral Characteristics

Table 3. Signal to Noise and Distortion (SINAD), Typical[15]

Frequency (MHz)	SINAD (dB), Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
1	64	66	63
10	61	60	47

Frequency (MHz)	SINAD (dB), Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
20	57	56	42
30	60	62	62
40	60	62	62
43	58	60	55

Table 4. Spurious-Free Dynamic Range (SFDR)[16] with Harmonics, Typical[17]

Frequency (MHz)	SFDR (dB) with Harmonics, Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
1	76	71	58
10	68	64	47
20	60	57	42
30	73	73	74
40	76	73	74
43	78	75	59

Table 5. SFDR without Harmonics, Typical[18]

Frequency (MHz)	SFDR (dB) without Harmonics, Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
1	87	90	90
10	86	88	90
20	79	88	88
30	72	72	73
40	75	72	73
43	77	74	59

Table 6. 0 °C to 40 °C Total Harmonic Distortion (THD) [19]

Frequency (MHz)	THD (dBc)		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
20 kHz	-77, typical	-77, typical	-77, typical
1 MHz	-75, typical	-70, typical	-62, typical
5 MHz	-68	-68	-55
10 MHz	-65	-61	-46

Frequency (MHz)	THD (dBc)		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
	-66, typical[20]	-66, typical[20]	
20 MHz	-55 -61, typical[20]	-53 -61, typical[20]	-40
30 MHz	-50 -57, typical[20]	-48 -57, typical[20]	-38
40 MHz	-47 -54, typical[20]	-46 -54, typical[20]	-34
43 MHz	-46 -53, typical[20]	-45 -53, typical[20]	-33

Table 7. 0 °C to 55 °C Total Harmonic Distortion (THD) [19]

Frequency (MHz)	THD (dBc)		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
20 kHz	-76, typical	-76, typical	-76, typical
1 MHz	-74, typical	-69, typical	-61, typical
5 MHz	-67	-67	-54
10 MHz	-63	-60	-45
20 MHz	-54 -57[20]	-52 -55[20]	-39
30 MHz	-48 -52[20]	-46 -50[20]	-36
40 MHz	-45 -50[20]	-41 -47[20]	-32
43 MHz	-44 -49[20]	-41 -46[20]	-31

Table 8. Average Noise Density[21]

Path	Amplitude Range		Average Noise Density		
	V_{pk-pk}	dBm	$\frac{nv}{\sqrt{Hz}}$ $\frac{nv}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
Direct	1	4.0	18	-142	-146.0
Low Gain	0.06	-20.4	9	-148	-127.6
	0.1	-16.0	9	-148	-132.0
	0.4	-4.0	13	-145	-141.0
	1	4.0	18	-142	-146.0
	2	10.0	35	-136	-146.0
High Gain	4	16.0	71	-130	-146.0
	12	25.6	213	-120	-145.6

Figure 4. 10 MHz Single-Tone Spectrum[22], Direct Path, 100 MS/s, DAC Interpolation Factor Set to 4

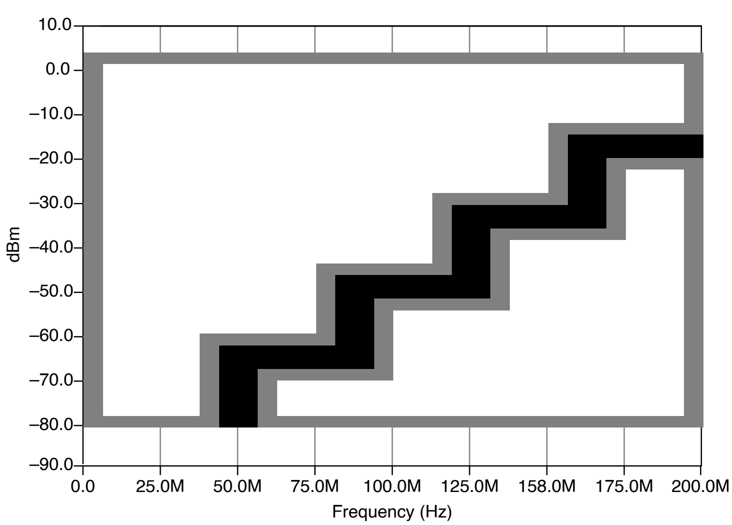


Figure 5. 10 MHz Single-Tone Spectrum[22], Low-Gain Amplifier Path, 100 MS/s, DAC Interpolation Factor Set to 4

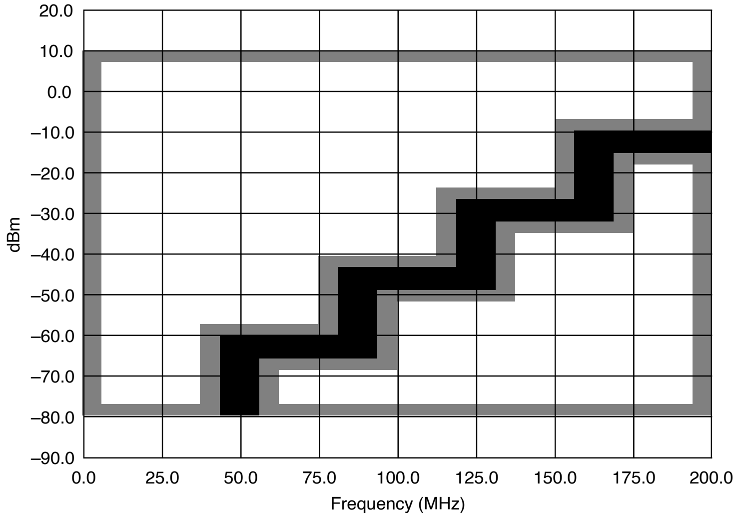
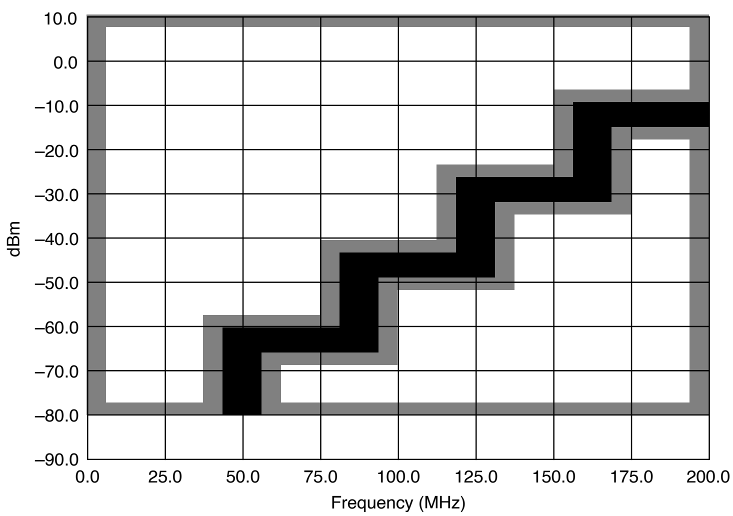


Figure 6. Direct Path, Two-Tone Spectrum[22], Typical



Sample Clock

Sample clock sources	Internal, Divide-by-**N** (**N** ≥ 1) Internal, DDS-based, high-resolution External, CLK IN (SMB front panel connector)

	External, DDC CLK IN (DIGITAL DATA & CONTROL front panel connector) External, PXI Star trigger (PXI backplane connector) External, PXI_Trig<0..7> (PXI backplane connector)

Sample Rate Range and Resolution

Sample Clock Source	Sample Rate Range	Sample Rate Resolution
Divide-by-**N**	23.84 S/s to 100 MS/s	Settable to (100 MS/s)/**N** (1 ≤ **N** ≤ 4,194,304)
High Resolution	10 S/s to 100 MS/s	1.06 µHz
CLK IN	200 kS/s to 105 MS/s	Resolution determined by external clock source. External sample clock duty cycle tolerance 40 to 60%.
DDC CLK IN	10 S/s to 105 MS/s	
PXI Star Trigger	10 S/s to 105 MS/s	
PXI_Trig<0..7>	10 S/s to 20 MS/s	

DAC Effective Sample Rate[23]

Sample Rate (MS/s)	DAC Interpolation Factor	Effective Sample Rate
10 S/s to 105 MS/s	1 (off)	10 S/s to 105 MS/s
12.5 MS/s to 105 MS/s	2	25 MS/s to 210 MS/s
10 MS/s to 100 MS/s	4	40 MS/s to 400 MS/s
10 MS/s to 50 MS/s	8	80 MS/s to 400 MS/s

Sample Clock Delay Range and Resolution

Sample Clock Source	Delay Adjustment Range	Delay Adjustment Resolution
Divide-by-**N**	±1 Sample clock period	<10 ps
High-Resolution	±1 Sample clock period	Sample clock period/16,384
External (all)	0 to 7.6 ns	<15 ps

System Phase Noise and Jitter (10 MHz Carrier)

Sample Clock Source	System Phase Noise Density[24] (dBc/Hz) Offset			System Output Jitter[24] (Integrated from 100 Hz to 100 kHz)
	100 Hz	1 kHz	10 kHz	
Divide-by-**N**	-110	-131	-137	<1.0 ps rms
High-Resolution[25]	-114	-126	-126	<4.0 ps rms
CLK IN	-113	-132	-135	<1.1 ps rms
PXI Star Trigger[26]	-115	-118	-130	<3.0 ps rms

External Sample Clock Input Jitter Tolerance

Cycle-cycle jitter	±300 ps
Period Jitter	±1 ns

Sample Clock Exporting

Exported Sample Clock Destinations[27]	PFI<0..1> (SMB front panel connectors) DDC CLK OUT (DIGITAL DATA & CONTROL front panel connector) PXI_Trig<0..6> (PXI backplane connector)

Destination	Maximum Frequency	Jitter, typical	Duty Cycle
PFI<0..1>	105 MHz	PFI 0: 6 ps rms PFI 1: 12 ps rms	25 to 65%
DDC CLK OUT	105 MHz	40 ps rms	40 to 60%
PXI_Trig<0..6>	20 MHz	—	—

Note Sample clock purity can significantly affect the performance of the PXI-5441. High amounts of jitter or phase noise in the sample clock can create spurs in the signal generator's spectrum that are not present when

> using a pure sample clock. For example, if the Clock Mode property is set to Automatic, NI-FGEN often selects High-Resolution clocking to achieve a specific IQ rate. High-Resolution clocking has more jitter than Divide-By-**N** clocking and may create extra spurs in the waveform generator output spectrum. To remove extra spurs without using software resampling, you can use a pure external clock such as the PXI-5650/5651/5652 frequency sources, with low jitter and <1 Hz frequency resolution.

Onboard Clock (Internal VCXO)

Clock Source	Internal sample clocks can either be locked to a reference clock using a phase-locked loop or be derived from the onboard VCXO frequency reference.
Frequency Accuracy	±25 ppm

Phase-Locked Loop (PLL) Reference Clock

Reference Clock Sources[28]	PXI_CLK10 (PXI backplane connector) CLK IN (SMB front panel connector)
Frequency Accuracy	When using the PLL, the frequency accuracy of the PXI-5441 is solely dependent on the frequency accuracy of the PLL reference clock source.
Lock Time	70 ms, typical 200 ms, maximum
Frequency Range	5 to 20 MHz in increments of 1 MHz. Default of 10 MHz. The PLL reference clock frequency must be accurate to ±50 ppm.
Duty Cycle Range	40 to 60%

Exported PLL Reference Clock Destinations	PFI<0..1> (SMB front panel connectors) PXI_Trig<0..6> (PXI backplane connector)

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Connector	SMB (jack)
Direction	Input
Destinations	Sample clock PLL reference clock
Frequency Range	1 to 105 MHz (sample clock destination and sine waves) 200 kHz to 105 MHz (sample clock destination and square waves) 5 to 20 MHz (PLL reference clock destination)
Input Voltage Range	Sine wave: 0.65 to 2.8 $V_{pk\text{-}pk}$ into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 to 2.8 $V_{pk\text{-}pk}$ into 50 Ω
Maximum Input Overload	±10 V
Input Impedance	50 Ω
Input Coupling	AC

TClk Synchronization

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

National Instruments TClk synchronization method and the NI-TClk instrument driver are used to align the Sample Clocks on any number of SMC-based modules in a chassis.

- Specifications are valid for any number of PXI modules installed in one PXI-1042 chassis
- All parameters are set to identical values for each SMC-based module
- Sample Clock is set to 100 MS/s, Divide-by-**N**, and all filters are disabled
- For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support

Skew[29]	500 ps, typical
Average skew after manual adjustment[30]	<10 ps, typical
Sample Clock delay/adjustment resolution	≤10 ps, typical

Note Although you can use NI-TClk to synchronize nonidentical modules, these specifications apply only to synchronizing identical modules.

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Connectors	Two SMB (jacks)
Direction	Bidirectional

Frequency Range	DC to 105 MHz

As an Input (Trigger)

Destinations	Start trigger
Maximum Input Overload	-2 to +7 V
V_{IH}	2.0 V
V_{IL}	0.8 V
Input Impedance	1 kΩ

As an Output (Event)

Sources	Sample clock divided by integer **K** (1 ≤ **K** ≤ 4,194,304) Sample clock timebase (100 MHz) divided by integer **M** (2 ≤ **M** ≤ 4,194,304) PLL reference clock Marker Exported start trigger (Out Start trigger)
Output Impedance	50 Ω
Maximum Output Overload	-2 to +7 V

V_{OH}[31]	Minimum: 2.9 V (open load), 1.4 V (50 Ω load)
V_{OL}[31]	Maximum: 0.2 V (open load), 0.2 V (50 Ω load)
Rise/Fall Time[32]	≤2.0 ns

DIGITAL DATA & CONTROL (DDC)

Optional Front Panel Connector

Connector type	68-pin VHDCI female receptacle
Number of Data Output Signals	16
Control signals	DDC CLK OUT (clock output) DDC CLK IN (clock input) PFI 2 (input) PFI 3 (input) PFI 4 (output) PFI 5 (output)
Ground	23 pins

Output Signal Characteristics (Includes Data Outputs, DDC CLK OUT, and PFI<4..5>)

LVDS (Low-Voltage Differential Signal)[33]

V_{OH}	1.3 V, typical
	1.7 V, maximum
V_{OL}	0.8 V, minimum
	1.0 V , typical
Differential Output Voltage	0.25 V , minimum
	0.45 V , maximum
Output Common-Mode Voltage	1.125 V , minimum
	1.375 V , maximum
Differential Pulse Skew (skew within a differential pair)	0.6 ns , maximum
Rise/Fall time	0.5 ns , typical
	1.6 ns , maximum

Output skew	Typical: 1 ns; maximum 2 ns. Skew between any two output terminals on the DIGITAL DATA & CONTROL front panel connector.
Output Enable/Disable	Controlled through the software on all data output signals and control signals collectively. When disabled, the output terminals go to a high-impedance state.

Maximum Output Overload	-0.3 to +3.9 V

Input Signal Characteristics (Includes DDC CLK IN and PFI<2..3>)

Signal type	LVDS (Low-Voltage Differential Signal)
Input Differential Impedance	100 Ω
Maximum Output Overload	-0.3 to +3.9 V
Signal Characteristics	
Differential Input Voltage	0.1 V, minimum
	0.5 V, maximum
Input Common Mode Voltage	0.2 V, minimum
	2.2 V, maximum

DDC CLK OUT

Clocking format	Data outputs and markers change on the falling edge of DDC CLK OUT.
Frequency Range	Refer to the **Sample Clock** section for more information
Duty cycle	40 to 60%
Jitter	40 ps rms

DDC CLK IN

Clocking format	DDC data output signals change on the rising edge of DDC CLK IN.
Frequency range	10 Hz to 105 MHz
Input Duty Cycle Tolerance	40 to 60%
Input Jitter Tolerances	300 ps pk-pk of cycle-cycle jitter, and 1 ns rms of period jitter.

Start Trigger

Sources	PFI<0..1> (SMB front panel connectors) PFI<2..3> (DIGITAL DATA & CONTROL front panel connector) PXI_Trig<0..7> (backplane connector) PXI Star trigger (backplane connector) Software (use function call) Immediate (does not wait for a trigger). Default.
Modes	Single Continuous Stepped Burst
Edge Detection	Rising

Minimum Pulse Width	25 ns

Table 9. Delay from Start Trigger to CH 0 Analog Output with OSP Disabled.

DAC Interpolation Factor	Typical Delay
Digital interpolation filter disabled	44 Sample clock periods + 110 ns
2	58 Sample clock periods + 110 ns
4	64 Sample clock periods + 110 ns
8	65 Sample clock periods + 110 ns

Delay from Start Trigger to Digital Data Output with OSP Disabled.	40 Sample clock periods + 110 ns
Additional Delay for Function Generator Mode	Add 33 Sample clock periods. (Applicable to delay from Start trigger to CH0 analog output and delay from Start trigger to digital data output)
Additional Delay with OSP Enabled[34]	Add 70 Sample clock periods for real data processing mode Add 73 Sample clock periods for complex data processing mode. (Applicable to delay from Start trigger to CH0 analog output and delay from Start trigger to digital data output)
Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the **Destinations** specification in the **Markers** section.
Exported Trigger Delay	65 ns, typical
Exported Trigger Pulse Width	>150 ns

Markers

Destinations	PFI<0..1> (SMB front panel connectors)

	PFI<4..5> (DIGITAL DATA & CONTROL front panel connector) PXI_Trig<0..6> (backplane connector)
Quantity	One marker per segment
Quantum	Marker position must be placed at an integer multiple of four samples (two samples for Complex (IQ) data).
Width	>150 ns

Table 10. Skew

Destination	With Respect to Analog Output	With Respect to Digital Data Output
PFI<0..1>	±2 Sample Clock Periods	N/A
PFI<4..5>	N/A	<2 ns
PXI_Trig<0..6>	±2 Sample Clock Periods	N/A

Jitter	20 ps rms

Arbitrary Waveform Generation Mode

Memory usage	The PXI-5441 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.

Onboard Memory Size

32 MB option	33,554,432 bytes
256 MB option	268,435,456 bytes
512 MB option	536,870,912 bytes

Output modes	Arbitrary Waveform mode and Arbitrary Sequence mode
Arbitrary Waveform Mode	In Arbitrary Waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.
Arbitrary Sequence Mode	In Arbitrary Sequence mode, a sequence directs the PXI-5441 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.

Table 11. Minimum Waveform Size (Samples)[35]

Trigger Mode	Arbitrary Waveform Mode	Arbitrary Sequence Mode
Single	16	16
Continuous	16	96 at >50 MS/s
		32 at ≤50 MS/s
Stepped	32	96 at >50 MS/s
		32 at ≤50 MS/s
Burst	16	512 at >50 MS/s
		256 at ≤50 MS/s

Loop count	1 to 16,777,215 Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of four samples (two samples for complex (IQ) data).

Table 12. Memory Limits[36]

	32 MB Option	256 MB Option	512 MB Option	Comments
Arbitrary Waveform Mode, Maximum	16,777,088 samples	134,217,600 samples	268,435,328 samples	For complex (IQ) data maximum waveform memory is halved.

	32 MB Option	256 MB Option	512 MB Option	Comments
Waveform Memory				
Arbitrary Sequence Mode, Maximum Waveform Memory	16,777,008 samples	134,217,520 samples	268,435,200 samples	Condition: One or two segments in a sequence. For complex (IQ) data maximum waveform memory is halved.
Arbitrary Sequence Mode, Maximum Waveforms	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	4,194,000 Burst trigger: 524,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Segments in a Sequence	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	6,708,000 Burst trigger: 4,180,000	Condition: Waveform memory is <4,000 samples. (<2,000 samples for complex (IQ) data.)

Table 13. Waveform Play Times [37]

	32 MB Option	256 MB Option	512 MB Option
Maximum Play Time, Sample Rate = 100 MS/s, OSP Disabled	0.16 seconds	1.34 seconds	2.68 seconds
Maximum Play Time, IQ Rate = 1 MS/s, Real Mode, OSP Enabled	16 seconds	2 minutes and 14 seconds	4 minutes and 28 seconds
Maximum Play Time, IQ Rate = 100 kS/s, Real Mode, OSP Enabled	2 minutes and 47 seconds	22 minutes and 22 seconds	44 minutes and 43 seconds

Function Generation Mode

Standard Waveforms and Maximum Frequencies	
Sine	43 MHz
Square	25 MHz
Triangle	5 MHz

Ramp Up	5 MHz
Ramp Down	5 MHz
DC	N/A
Noise (Pseudo-Random)	5 MHz
User Defined	43 MHz

Memory Size[38]	65,536 samples for 1/4 symmetric waveforms (Example: Sine) 16, 384 samples for non-1/4 symmetric waveforms (Example: Ramp)
Frequency Resolution	355 nHz
Phase Resolution	0.0055°

Onboard Signal Processing (OSP)

IQ Rate

OSP Interpolation Range[39]	12 to 512 (multiples of 2) 512 to 1,024 (multiples of 4) 1,024 to 2,048 (multiples of 8) (OSP Interpolation = FIR Interpolation x CIC Interpolation)
IQ Rate[40]	Sample rate/OSP interpolation (Lower IQ rates are possible by either lowering the sample rate or doing software interpolation)

Data Processing Modes	Real (I path only) Complex (IQ)

Prefilter Gain and Offset

Prefilter Gain and Offset Resolution	18 bits
Prefilter Gain Range[41]	-2.0 to +2.0 (Values < |1| attenuate user data)
Prefilter Offset Range[42]	-1.0 to +1.0
Output[43]	(User data x Prefilter gain) + Prefilter offset(-1 ≤ output ≤ +1)

FIR (Finite Impulse Response) Filter The FIR filter is used to pulse shape the IQ data and to compensate for the CIC filter roll-off.

Filter Length	95 Taps
Coefficient Width	17 bits (-1 to +1)
Filter Symmetry	Symmetric
Interpolation Range	2, 4, or 8
Coefficients	Automatically generated by NI-FGEN (refer to **FIR Filter Types**) or Custom Coefficients provided by the user

Table 14. FIR Filter Types

Type	Parameter	Minimum	Maximum
Custom[44]	-	-	-
Flat[45]	Passband	0.1	0.43
Gaussian	BT	0.1	0.9
Raised Cosine	Alpha	0.1	0.9
Root Raised Cosine	Alpha	0.1	0.9

CIC (Cascaded Integrator-Comb) Filter The CIC Filter does the majority of the interpolation in the OSP.

Size	6 stages
Interpolation Range	6 ≤ Interpolation ≤ 256 (integers)

Numerically Controlled Oscillator (NCO)

Frequency Range	1 mHz to (0.43 x sample rate)
Frequency Resolution[46]	Sample rate / 2^{48}
I and Q Phase Resolution	0.0055°
Phase Quantization[47]	16 bits
Tuning Speed	1 ms

Table 15. Modulation Performance, Typical [48]

Modulation Configuration	Measurement Type	FIR Interpolation		
		2	4	8
GSM Physical Layer[49]	MER (Modulation Error Ratio)	46 dB	47 dB	42 dB
	EVM (Error Vector Magnitude)	<0.5% rms	<0.5% rms	<0.8% rms
W-CDMA Physical Layer[50],[51]	MER	46 dB	39 dB	—
	EVM	<7 0.5 % rms	<1.0% rms	—
	ACPR (Adjacent Channel Power Ratio) (External Sample Clock)	65 dBc	68 dBc	—
	ACPR (High-Resolution Sample Clock)	61 dBc	61 dBc	—
DVB Physical Layer[52],[53]	MER	43 dB	—	—
	EVM	<0.6% rms	—	—
	ACPR (Adjacent Channel Power Ratio) (External Sample Clock)	48 dBc	—	—
	ACPR (High-Resolution Sample Clock)	47 dBc	—	—

Digital Performance

Maximum NCO Spur[54]	<-90 dBc

FIR Interpolation[55]	IQ Rate Range (with 100 MS/s Sample Clock Rate)	OSP Out of Band Suppression	OSP Passband Ripple
2	195 kS/s to 8.33 MS/s	63 dB	0 to -0.08 dB
4	97.6 kS/s to 4.16 MS/s	74 dB	0 to -0.08 dB
8	48.8 kS/s to 2.08 MS/s	40 dB	0 to -0.08 dB

Figure 7. GSM Physical Layer[56] External Sample Clocking = 99.665 MHz

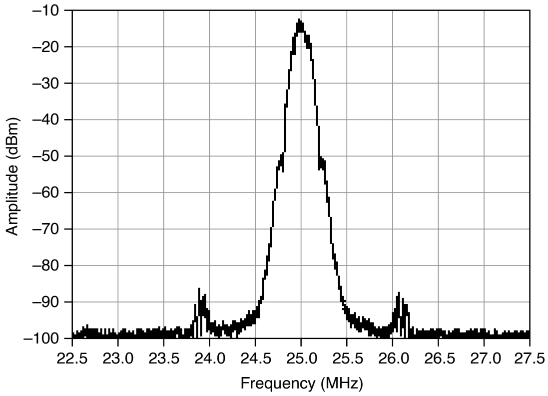


Figure 8. GSM Physical Layer[56][57] Internal (High Resolution) Sample Clocking = 99.665 MHz

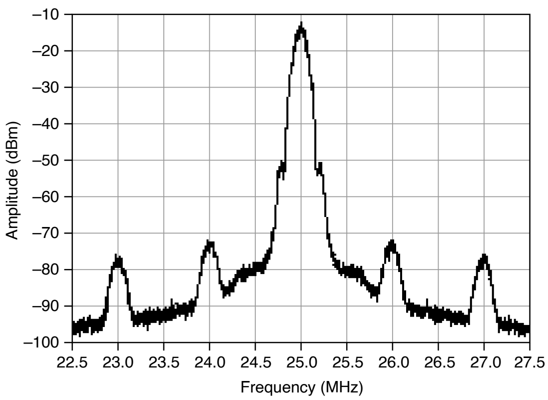


Figure 9. CDMA 2000 Physical Layer[58] External Sample Clocking = 98.304 MHz

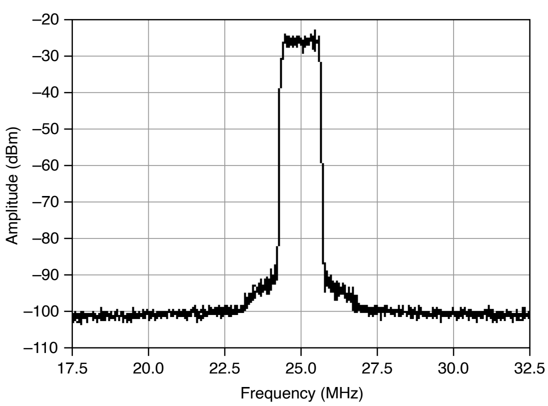


Figure 10. CDMA 2000 Physical Layer [58][57] Internal (High Resolution) Sample Clocking = 98.304 MHz

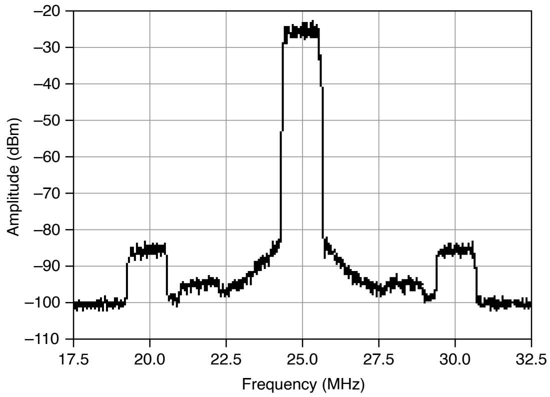


Figure 11. W-CDMA Physical Layer[59] External Sample Clocking = 92.16 MHz

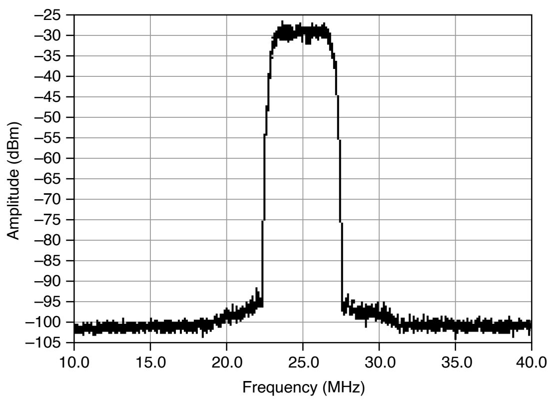


Figure 12. W-CDMA Physical Layer [59][57] Internal (High Resolution) Sample Clocking = 92.16 MHz

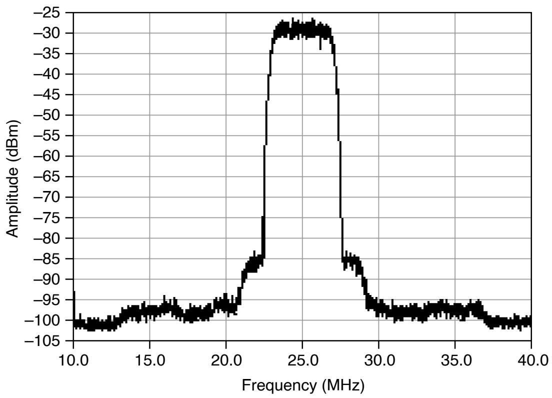


Figure 13. DVB Physical Layer[60][61] External Sample Clocking = 96.88 MHz

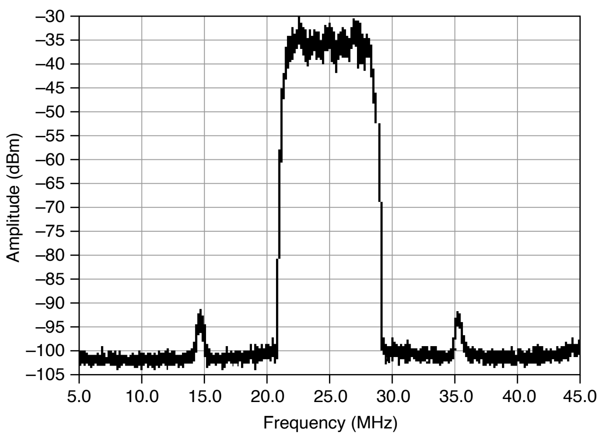
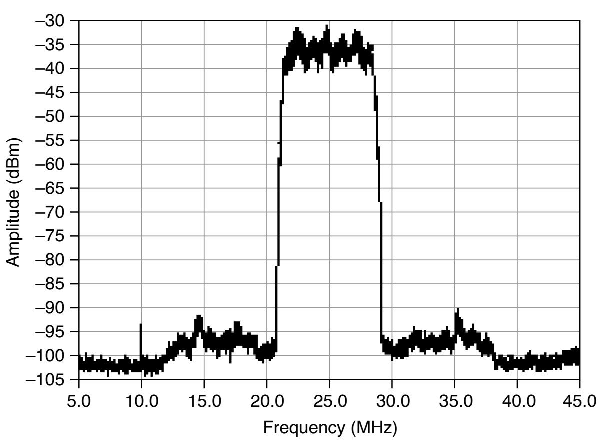


Figure 14. DVB Physical Layer[60][62][57] Internal (High Resolution) Sample Clocking = 96.88 MHz



Calibration

Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.
External Calibration	The external calibration calibrates the VCXO, voltage reference, output impedance, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.
Calibration Interval	Specifications valid within 2 years of external calibration
Warm-up Time	15 minutes

Power

+3.3 VDC	
Typical operation	1.9 A, typical
Overload operation[63]	2.7 A, typical
+5 VDC	
Typical operation	2.2 A, typical
Overload operation[63]	2.4 A, typical
+12 VDC	
Typical operation	0.46 A, typical

Overload operation[63]	0.5 A, typical
-12 VDC	
Typical operation	0.01 A, typical
Overload operation[63]	0.01 A, typical
Total	
Typical operation	22.9 W, typical
Overload operation[63]	27.0 W, typical

Physical

Dimensions	3U, one-slot, PXI/cPCI module[64] 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)
Weight	345 g (12.1 oz)

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) 0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) when installed in a PXI-101**x** or PXI-1000B chassis
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-25 °C to 85 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Shock

Operating[65]	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Storage	50 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)

Random vibration

Operating[65]	5 Hz to 500 Hz, 0.31 g_{rms} (Tested in accordance with IEC 60068-2-64.)

Nonoperating	5 Hz to 500 Hz, 2.46 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

1 Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used. NI-FGEN compensates for user-specified resistive loads.

2 Not available on the Direct Path.

3 The maximum output voltage of the PXI-5441 is determined by the amplitude range and the offset range.

4 For DC accuracy, **amplitude range** is defined as 2x the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, its DC accuracy is calculated by the following equation: ±0.2% * (16 V) ± 0.05% * (1.5 V) ± 500 µV = ±33.25 mV. All paths are calibrated for amplitude and gain errors. The Low-Gain and High-Gain Amplifier paths also are calibrated for offset errors.

5 50 kHz sine wave.

6 Measured at -3 dB.

7 The digital filter is not available for use for Sample clock rates below 10 MS/s. Refer to the DAC Effective Sample Rate section for more information about the effect of DAC interpolation on sample rates and the Onboard Signal Processing (OSP) section for more information about OSP interpolation.

8 Available only on Low-Gain amplifier and High-Gain amplifier Paths.

9 With respect to 50 kHz.

10 Analog filter and DAC Interpolation filter disabled.

11 Specifications apply only to E-revision and later PXI-5441 devices (National Instruments part number 191789E-0x)

12 Above 50 MHz, the response is the image response.

13 Disable the Analog filter and the DAC Interpolation filter for square, ramp, and triangle. The minimum frequency is 0 Hz.

14 Direct path is optimized for the frequency domain.

15 Amplitude -1 dBFS. Measured from DC to 50 MHz. SINAD at low amplitudes is limited by a -148 dBm/Hz noise floor.

16 Dynamic range is defined as the difference between the carrier level and the largest spur.

17 Amplitude -1 dBFS. Measured from DC to 50 MHz. Also called harmonic distortion. SFDR with harmonics at low amplitudes is limited by a -148 dBm/Hz noise floor. All values include aliased harmonics.

18 Amplitude -1 dBFS. Measured from DC to 50 MHz. SFDR without harmonics at low amplitudes is limited by a -148 dBm/Hz noise floor. All values include aliased harmonics.

19 Amplitude -1 dBFS. Includes the 2nd through the 6th harmonic.

20 Specifications apply only to E-revision and later PXI-5441 devices (National Instruments part number 191789E-0x).

21 Average Noise Density at small amplitudes is limited by a -148 dBm/Hz noise floor.

22 The noise floor is limited by the measurement device. Refer to the Average Noise Density specifications for more information about this limit.

23 DAC Effective Sample Rate = (DAC Interpolation factor) * (Sample Rate). Refer to the Onboard Signal Processing (OSP) section for OSP interpolation information.

[24] Specified at 2x DAC oversampling.

[25] High-Resolution specifications increase as the sample rate is decreased .

[26] PXI star trigger specification is valid when the sample clock source is locked to PXI_CLK10.

[27] Exported sample clocks can be divided by integer **K** (1 ≤ **K** ≤ 4,194,304).

[28] The PLL reference clock provides the reference frequency for the PLL.

[29] Caused by clock and analog path delay differences. No manual adjustment performed.

[30] For information about manual adjustment, search ni.com for NI-TClk Synchronization Repeatability Optimization or for help with the adjustment process, contact NI Technical Support at ni.com/support.

[31] Output drivers are +3.3 V TTL compatible.

[32] Load of 10 pF

[33] Tested with 100 Ω differential load. Measured at the device front panel. Load capacitance <15 pF. Driver and receiver comply with ANSI/TIA/ EIA-644.

[34] FIR and CIC filters enabled

[35] The minimum waveform size is sample rate dependent in Arbitrary Sequence mode. For complex (IQ) data minimum waveform size is halved.

[36] All trigger modes except where noted.

[37] Single Trigger mode. Play times can be significantly extended by using Continuous, Stepped, or Burst Trigger modes. For Complex (IQ) mode the play times are halved

[38] 16-bit samples. User Defined Waveforms must be exactly 16,384 samples.

39 Total PXI-5441 interpolation = OSP interpolation x DAC interpolation

40 Example: For a Sample rate of 100 MS/s, IQ rate range = 48.8 kS/s to 8.3 MS/s

41 Unitless

42 Applied after Prefilter gain

43 Prefilter output

44 Coefficients are provided by the user.

45 Lowpass filter that minimizes ripple to IQ rate x Passband.

46 Example: 355 nHz with a sample rate of 100 MS/s

47 Look-up table address width

48 Direct path (4 dBm peak), 25 MHz carrier

49 OSP Enabled. IQ Rate = 1.083 MS/s, 4 Samples/Symbol. FIR Filter Type = Flat, Passband = 0.4. MSK modulation. Software Pulse Shaping and Phase Accumulation, 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 14.

50 OSP Enabled. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.22. QPSK. PN Sequence Order = 15.

51 ACPR Measurement BW = 4 MHz and Channel Spacing = 5 MHz

52 OSP Enabled. IQ Rate = 6.92 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.15. 32 QAM modulation. PN Sequence Order = 15

53 ACPR Measurement BW = 7.96 MHz and Channel Spacing = 8 MHz

54 Full-scale output

55 FIR Filter Type = Flat. Passband = 0.4. Ripple Measurement to 0.4 x IQ Rate. Stop Band Suppression from 0.6 x IQ Rate.

[56] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 1.083 MS/s, 4 Samples/Symbol. FIR Filter Type = Flat, Passband = 0.4. Software MSK modulation: 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 14. For more information about eliminating spurs, refer to the DAC Effective Sample Rate section.

[57] Additional artifacts are caused by High Resolution Clock spurs.

[58] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 1.2288 MS/s, 1 Sample/Symbol. FIR Filter Type = Custom Flat Filter with Passband = 0.48. QPSK. PN Sequence Order = 15. For more information about eliminating spurs, refer to the DAC Effective Sample Rate section.

[59] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root Raised Cosine, Alpha = 0.22. QPSK. PN Sequence Order = 15. For more information about eliminating spurs, refer to the DAC Effective Sample Rate section.

[60] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 6.92 MS/s, 1 Sample/Symbol. FIR Filter Type = Root Raised Cosine, Alpha = 0.15. 32 QAM Modulation. PN Sequence Order = 15. For more information about eliminating spurs, refer to the DAC Effective Sample Rate section.

[61] Artifacts at 15 MHz and 35 MHz are due to 2x FIR Interpolation aliasing.

[62] Artifact at 10 MHz is caused by CLK IN feed-through.

[63] Overload operation occurs when CH 0 is shorted to ground.

[64] PXI-5441 modules of revision B and later are equipped with a modified PXI Express-compatible backplane connector. This modified connector allows the PXI-5441 to be supported by hybrid slots in a PXI Express chassis. To determine the revision of an PXI-5441 module, read the label on the underside of the PXI-5441. The label will list an assembly number of the format 191789**x**-01, where **x** is the revision.

[65] Spectral and jitter specifications could degrade.